Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM29F08I3/FM29LF08I3
8G-BIT NAND FLASH MEMORY

Datasheet

Aug. 2024

Trademarks

Features Summary

- **Single-level cell(SLC) technology**
- **ONFI 1.0 Compliant**
- **Voltage Supply**
  - 2.7V ~ 3.6V
  - 1.7V ~ 1.95V
- **Memory Cell Organization**
  - Page Size:
    X8: 4K+256 bytes
  - Block Size: 64 Pages
    X8: 256K+16K bytes
  - Plane Size: 2048 Blocks
  - 2 Device: 4GbX2
- **Page Read / Program Time**
  - Random Read Time: 30us (Max.)
  - Sequential Access time:
    3.3V Device: 25ns
    1.8V Device: 30ns
- **Program/Erase/Read Speed**
  - Page Program time : 400us (Typ.)
  - BLOCK ERASE time : 4ms (Typ.)
- **Command/Address/Data Multiplexed I/O Port**
- **Hardware Data Protection**
  - Program/Erase Lockout during Power Transitions
- **Reliability**
  - Endurance : 100K Program/Erase Cycles
  - Data retention: 10 years
- **ECC Requirement**
  - 8bit/512 byte
- **Command Driven Operation**
- **Package**
  - TSOP48 (12X20mm)
  - FBGA63 (9X11mm)
  - All Packages are RoHS Compliant and Halogen-free

1. Summary Description

FM29F08I3/FM29LF08I3 is a **1G**x8bit with spare **64M**x8(x8) bit capacity.
The device is offered in 3.3/1.8 Vcc Power Supply, and with x8 I/O interface.
The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains **4096** blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells.
Memory array is split into 2 die and one die consisting of **2048** blocks.
Program operation allows the **4352**-byte page writing in typical 400us and an erase operation can be performed in typical 4ms on a **256K**-byte block.
Data in the page can be read out at 20ns cycle time per byte (3.3V version), and at 30ns cycle time per byte (1.8V version). The I/O pins serves as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.
Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.
The on-chip Program/Erase controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using WP# input pin.
This device supports ONFI 1.0 specification.
The output pin R/B# (open drain) signals the status of the device during program/erase/read operation. In a system with multiple memories the R/B# pins can be connected all together to provide a global status signal.
The FM29F08I3/FM29LF08I3 is available in the following packages : 48-TSOP 12X20 mm package and FBGA63 9X11mm.

1.1. Product List

Part Number	Organization	Vcc range	Package
FM29F08I3	X8	2.7 - 3.6V	TSOP48, BGA63
FM29LF08I3	X8	1.7 - 1.9V	TSOP48, BGA63

1.2. Package

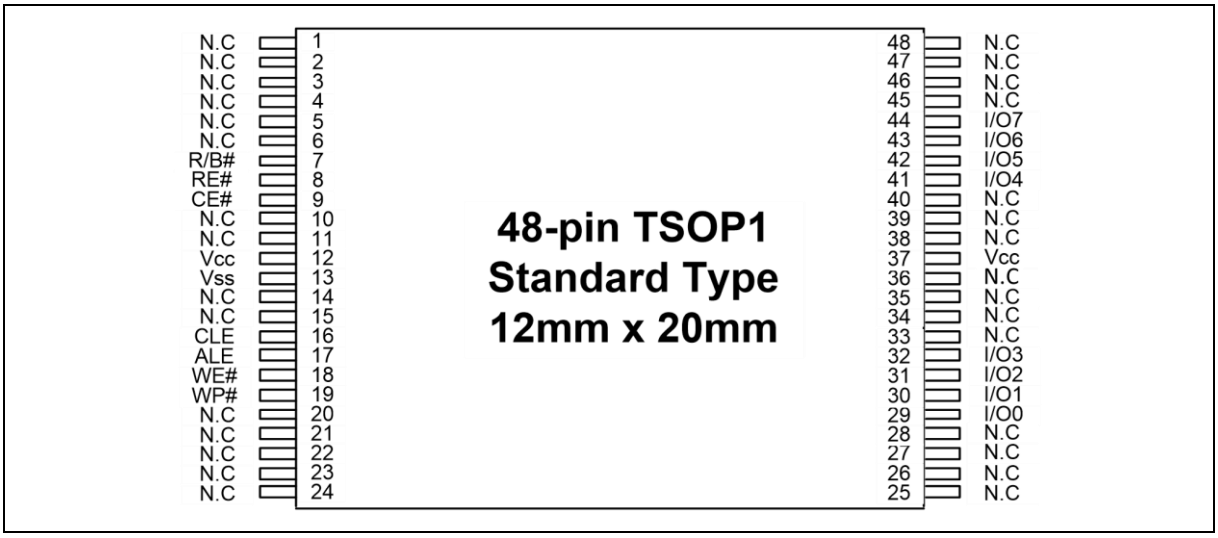


Figure 1 FM29F08I3/FM29LF08I3 pad assignments, TSOP48

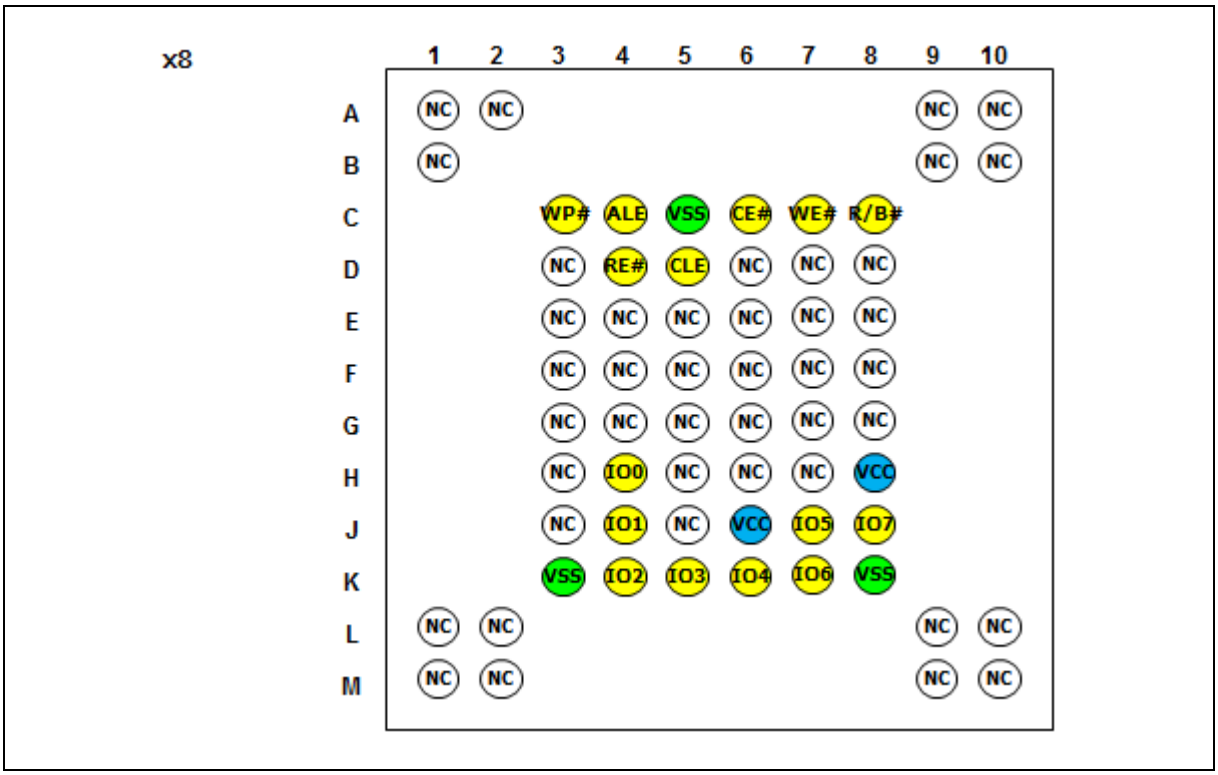


Figure 2 FM29F08I3/FM29LF08I3 ball assignments, FBGA63

1.3. Pin Description

Pin Name	FUNCTION
I/O0~I/O7	Data Inputs/Outputs The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	Command Latch Enable The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE# signal.
ALE	Address Latch Enable The ALE input controls the activating path for address to the internal address register. Addresses are latched on the rising edge of WE# with ALE high.
CE#	Chip Enable The CE# input is the device selection control. When the device is in the Busy State, CE# high is ignored, and the device does not return to standby mode in program or erase operation.
RE#	Read Enable The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WE#	Write Enable The WE# input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	Write Protect The WP# pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	Ready/Busy Output The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
Vcc	Power Vcc is the power supply for device.
Vss	Ground
N.C	No connection Lead is not internally connected.

Note:

1. A 0.1uF capacitor should be connected between the VCC supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB tracks widths must be sufficient to carry the currents required during program and erase operations.

1.4. Block Diagram

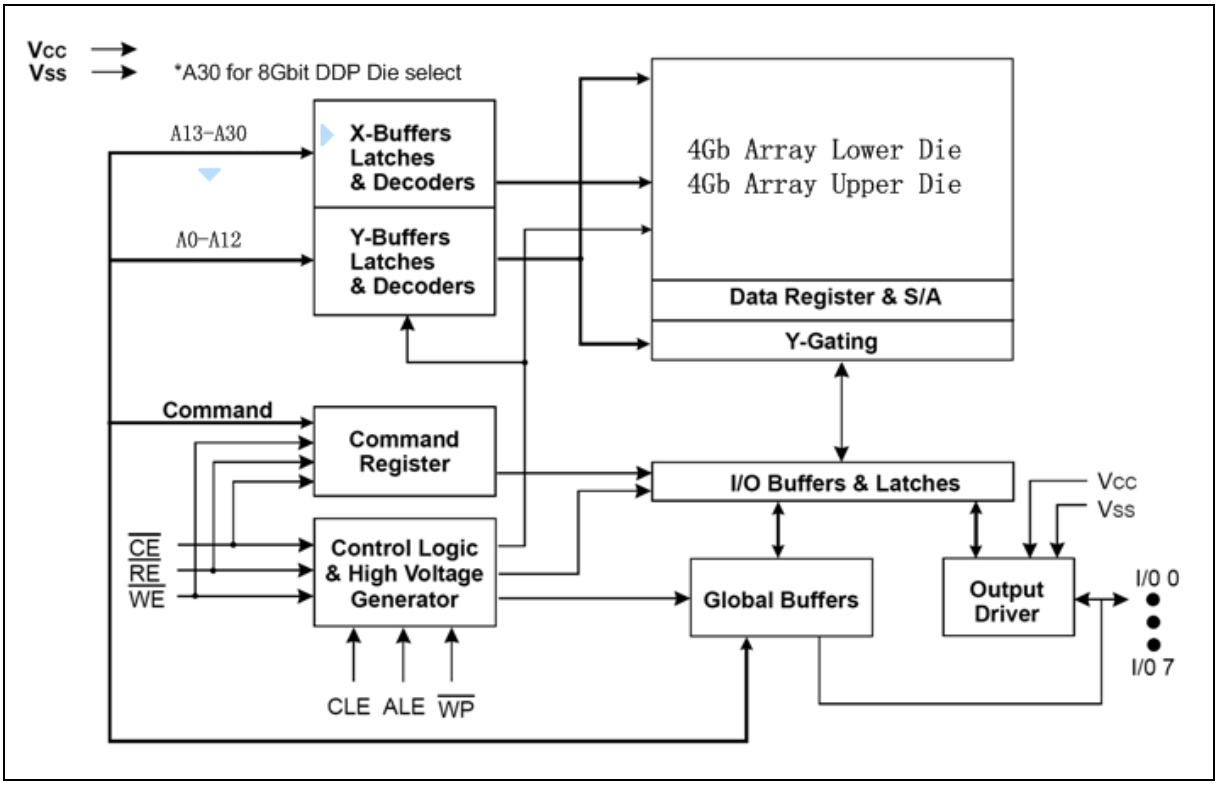


Figure 3 FM29F08I3/FM29LF08I3 NAND Flash Memory Block Diagram

1.5. Memory Mapping

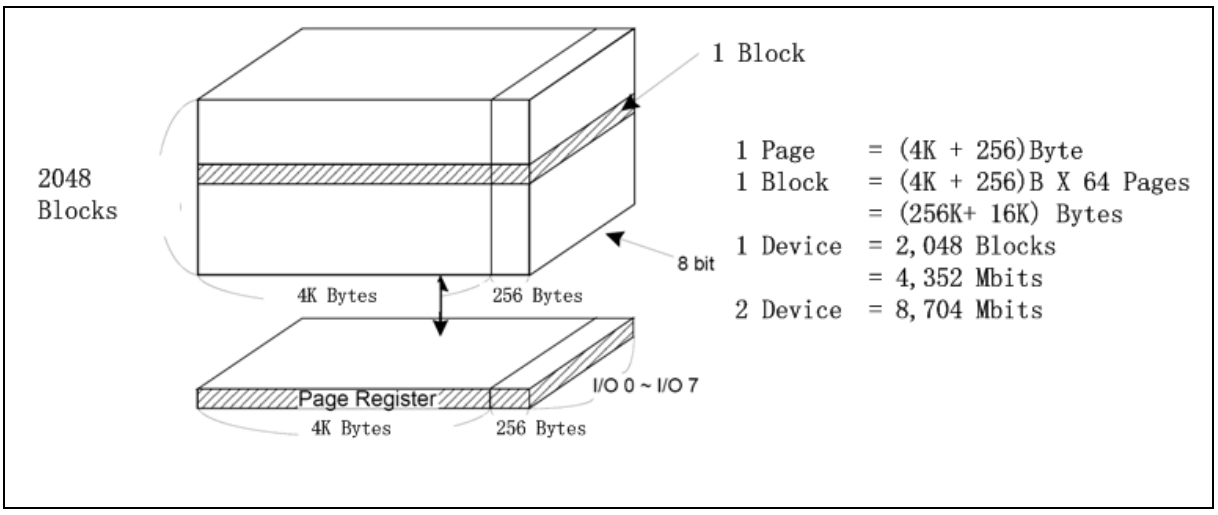


Figure 4 FM29F08I3/FM29LF08I3 Memory Map

1.6. Address role

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	A12	0	0	0
3rd Cycle	A13	A14	A15	A16	A17	A18	A19	A20
4th Cycle	A21	A22	A23	A24	A25	A26	A27	A28
5th Cycle	A29	A30	0	0	0	0	0	0

NOTE:

1. A30 for 8Gbit DDP Die select.

A0 - A12 : byte (column) address in the page

A13 - A18 : page address in the block

A19 - A30 : block address

1.7. Command Set

Function	1st Cycle	2nd Cycle	Accept Command during Busy
Read	00h	30h	
Read for copy back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	Yes
Page PGM	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Read Status	70h		Yes
Read Status Enhanced	78h		Yes
Random Data Input(1)	85h	-	
Random Data Output(1)	05h	E0h	
Read Parameter Page	ECh	-	
Read Unique ID	EDh	-	

Table 1 Command Sets

NOTE:

1. Random Data Input/Output can be executed in a page.

Caution: Any undefined command inputs are prohibited except for above command set of Table 1.

2. Bus Operation

The bus on the device is multiplexed. Data IO, addresses and commands all share the same pins.

The command sequence typically consists of a COMMAND LATCH cycle, address input cycles, and one or more data cycles, either READ or WRITE.

There are serial standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Mode		CLE	ALE	CE#	WE#	RE#	WP#
Read Mode	Command Input	H	L	L	Rising	H	X
	Address Input	L	H	L		H	X
Write Mode	Command Input	H	L	L		H	H
	Address Input	L	H	L		H	H
Data Input		L	L	L		H	H
Data Output		L	L	L	H	Falling	X
During Read (Busy)		X	X	X	X	H	X
During Program (Busy)		X	X	X	X	X	H
During Erase (Busy)		X	X	X	X	X	H
Write Protect		X(1)	X	X	X	X	L
Stand-by		X	X	H	X	X	0V/Vcc(2)

NOTE:

1. X can be VIL or VIH.
2. WP# should be biased to CMOS high or CMOS low for standby.

2.1. Command Latch Cycle

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover, for commands that starts a modify operation (write/erase) the Write Protection pin must high.

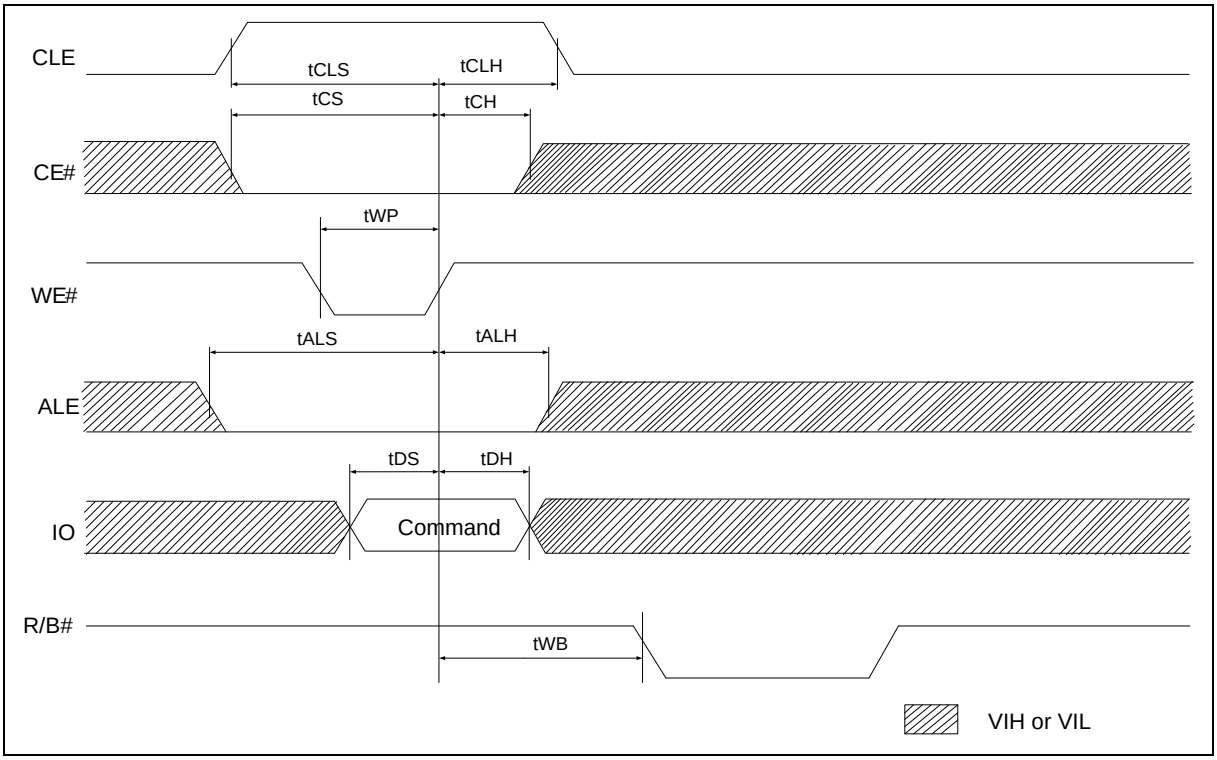


Figure 5 Command Latch timing

2.2. Address Latch Cycle

Address Input bus operation allows the insertion of the memory address. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable.

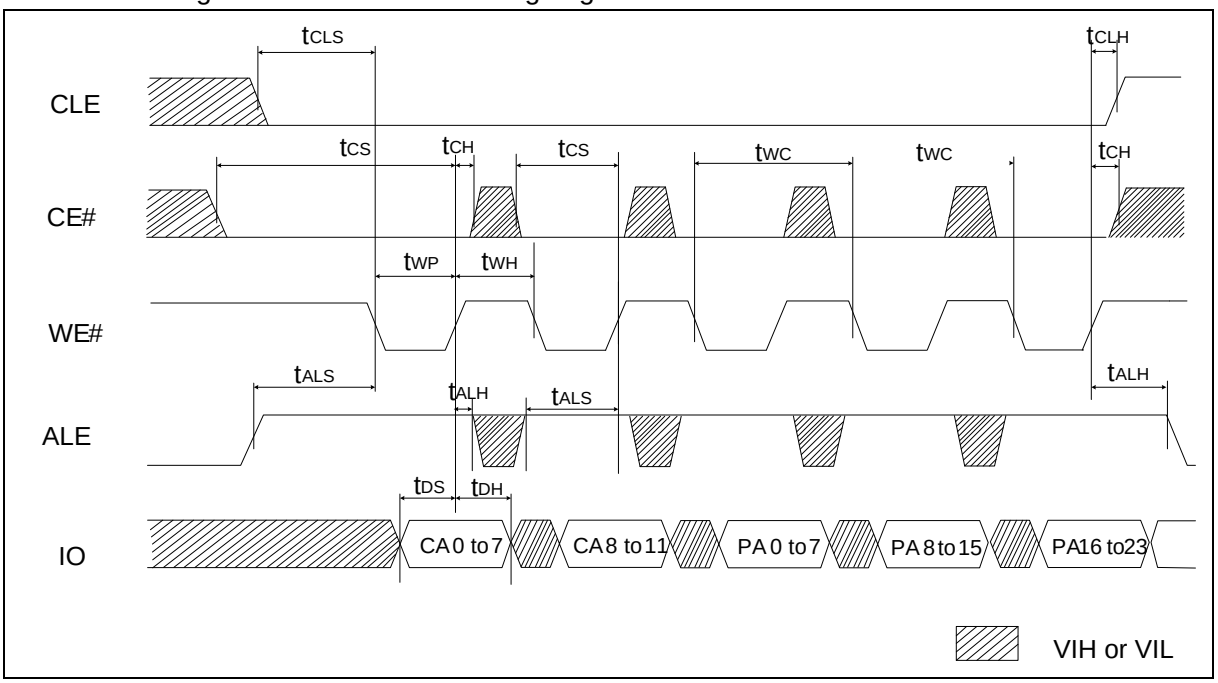


Figure 6 Address Latch timing

2.3. Input Data Latch Cycle

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low and Read Enable High, and Write Protect High and latched on the rising edge of Write Enable.

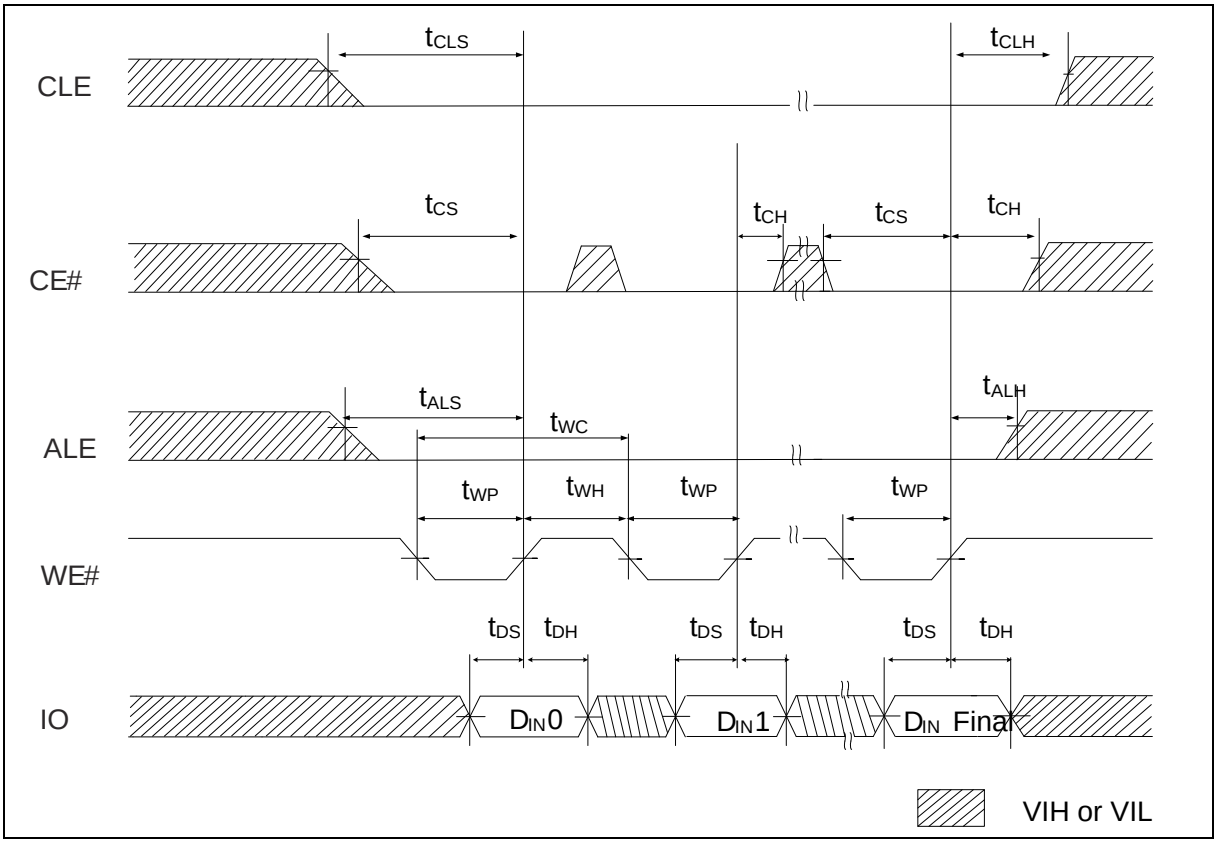
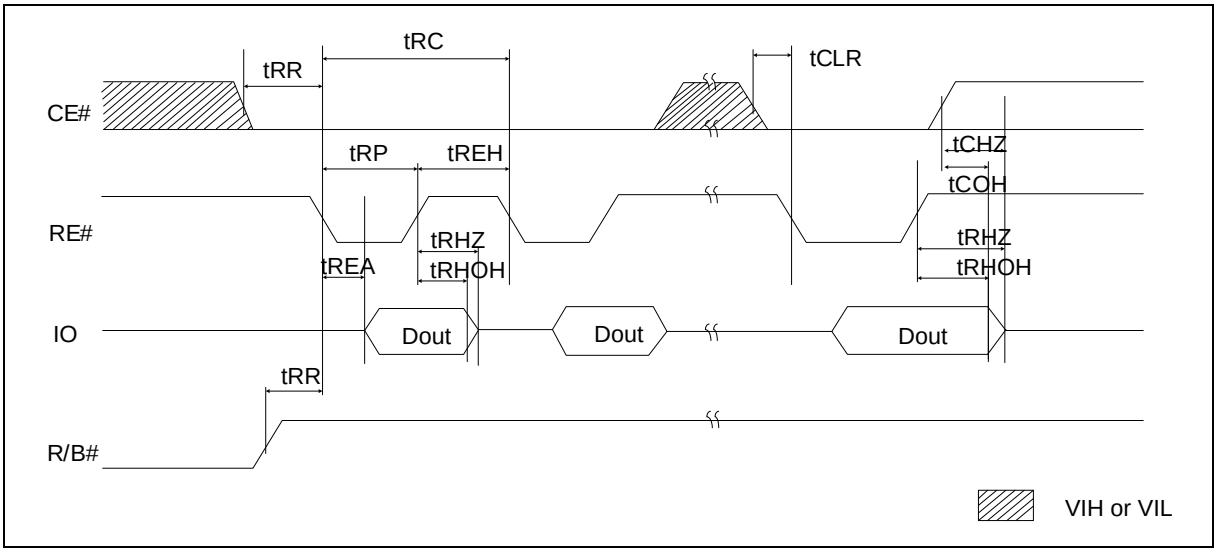


Figure 7 Input Data Latch timing

2.4. Serial Access Cycle after Read（CLE=L，WE#=H，ALE=L）

Data Output bus operation allows to output data from the device. The data output cycle is serially and timed by the Read Enable cycles. Data output may be used with CE# don't care. However, if CE# don't care is used t_{CEA} and t_{COH} timing requirements shall be met by the host.



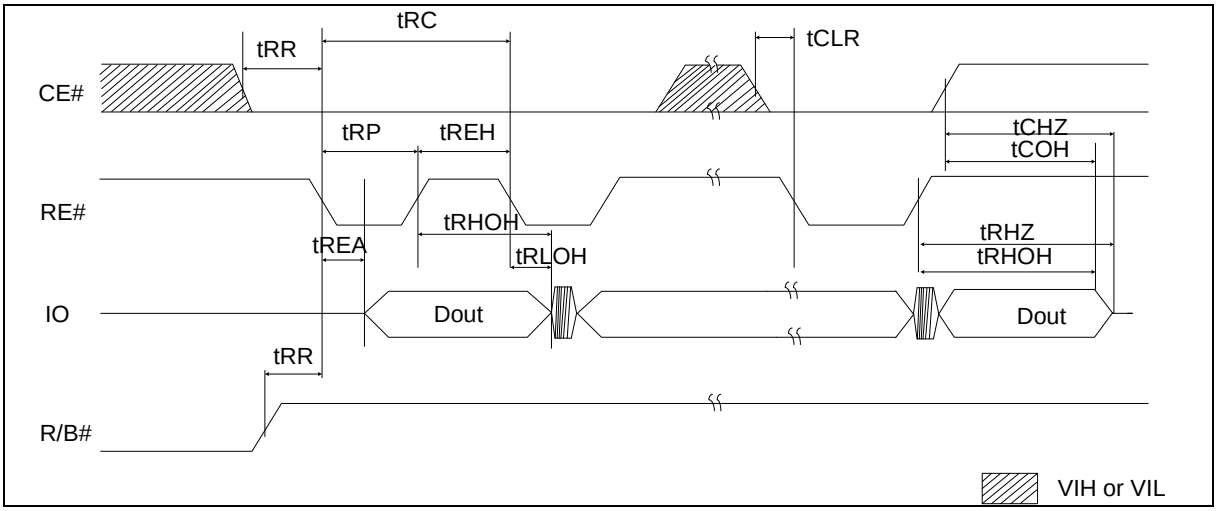
NOTES:

1. Transition is measured at ±200mV from steady state voltage with load.
2. This parameter is sampled and not 100% tested.
3. t_{RLOH} is valid when frequency is higher than 33MHz.
4. t_{RHOH} starts to be valid when frequency is lower than 33MHz.

Figure 8 Serial Read timing

2.5. Serial Access Cycle after Read（EDO Type, CLE=L，WE#=H，ALE=L）

If the host uses a sequential access time (tRC) of less than 30ns, the data can be latched on the next falling edge of RE# as the waveform of EDO mode.



NOTES:

1. Transition is measured at ±200mV from steady state voltage with load.
2. This parameter is sampled and not 100% tested.
3. t_{RLOH} is valid when frequency is higher than 33MHz.
4. t_{RHOH} starts to be valid when frequency is lower than 33MHz.

Figure 9 Serial Read timing with EDO mode

2.6. Write Protect

The Program and Erase Operations are automatically reset when WP# goes low. The operations are disabled and enabled as follows.

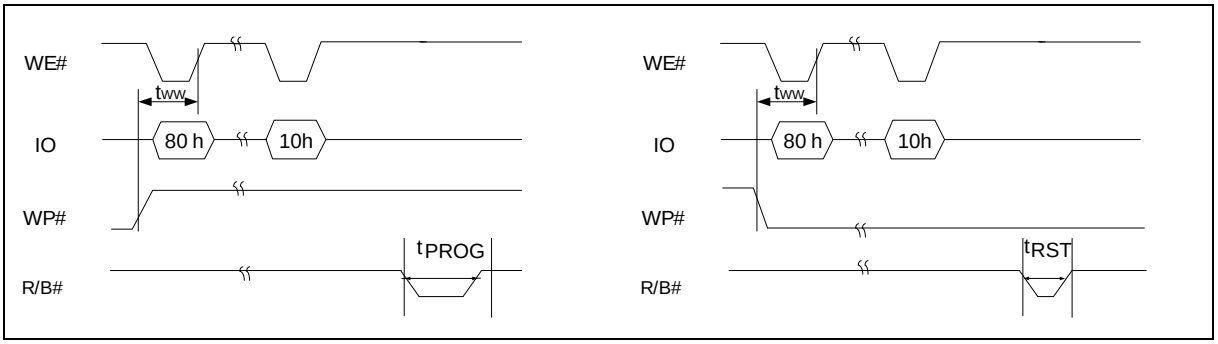


Figure 10 Write Protect Disable and Enable with Program

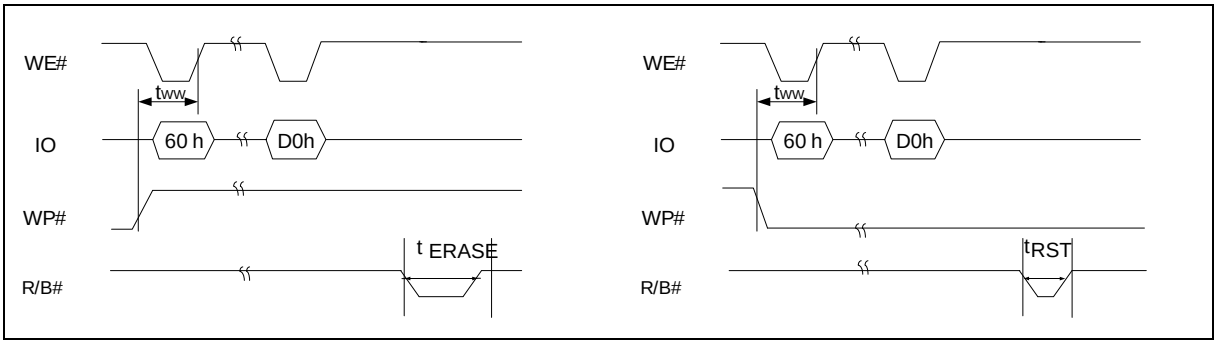


Figure 11 Write Protect Disable and Enable with Erase

3. Device Operations

3.1. Page Read Operation

3.1.1. Common Page Read (00H-30H)

Page read is initiated by writing 00h-30h to the command register along with five address cycles. The **4,352** bytes of data within the selected page are transferred to the cache registers in less than 30μs (t_R).

The system controller can detect the completion of his data transfer (t_R) by analyzing the output of R/B# pin or read status. Once the data in a page is loaded into the cache registers, they may be read out in t_{RC} cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.

After power up, device is in read mode so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode.

After the last data has been read out, CE# may be pulled up for some time to end the read operation, while during the RE# toggle cycle, CE# may be don't care when RE# is high. The CE# Don't care feature may simplify the system interface, which allows controller to directly download the code from flash device, and the CE# transitions will not stop the read operation during the latency time.

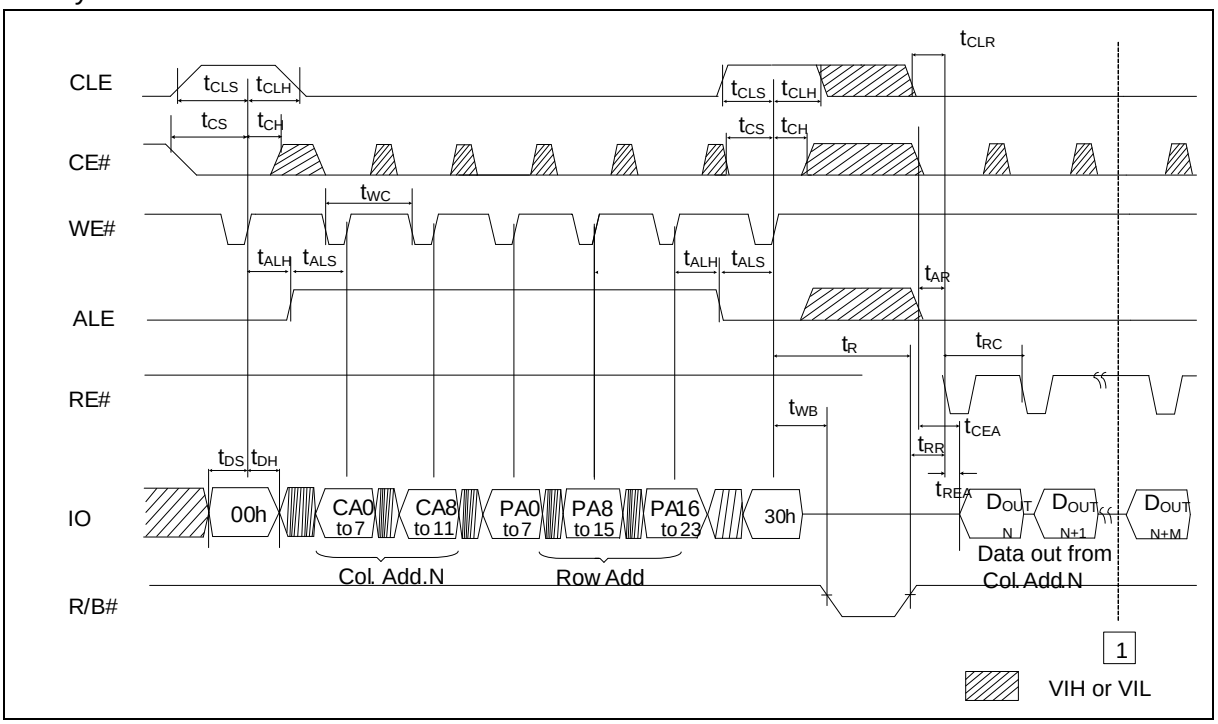


Figure 12 Read Operation

3.1.2. Random Data Output (05H-E0H)

The device may output random data in a page instead of the consecutive data by writing random data output command (05h-E0h). The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page. Random data output shall be issued when the device is in a read idle condition.

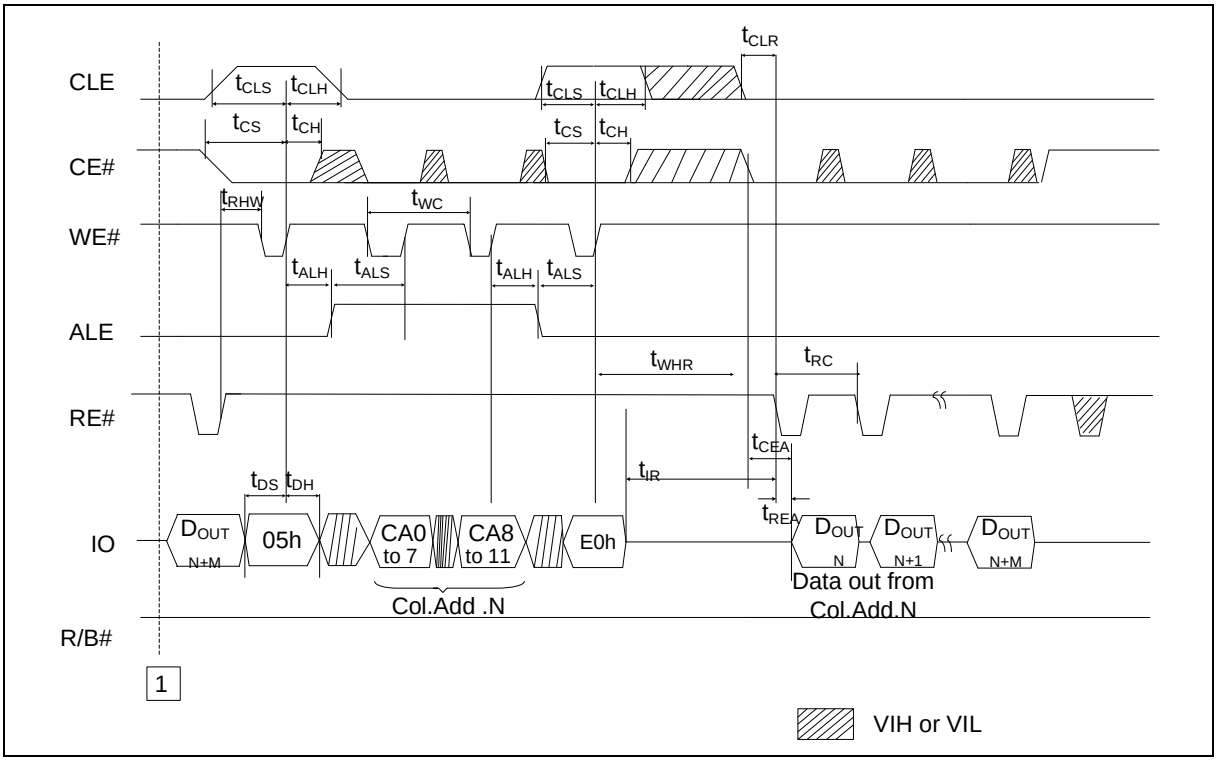


Figure 13 Random Data Output In a Page

3.1.3. Read for copy back(00h-35h)

The Copy-Back Read is configured to efficiently rewrite data stored in a page without data reloading when no error within the page is found. The data is read out only at page buffer for copy-back program.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the Copy-Back Program (85h-10h) command to prevent the propagation of data errors.

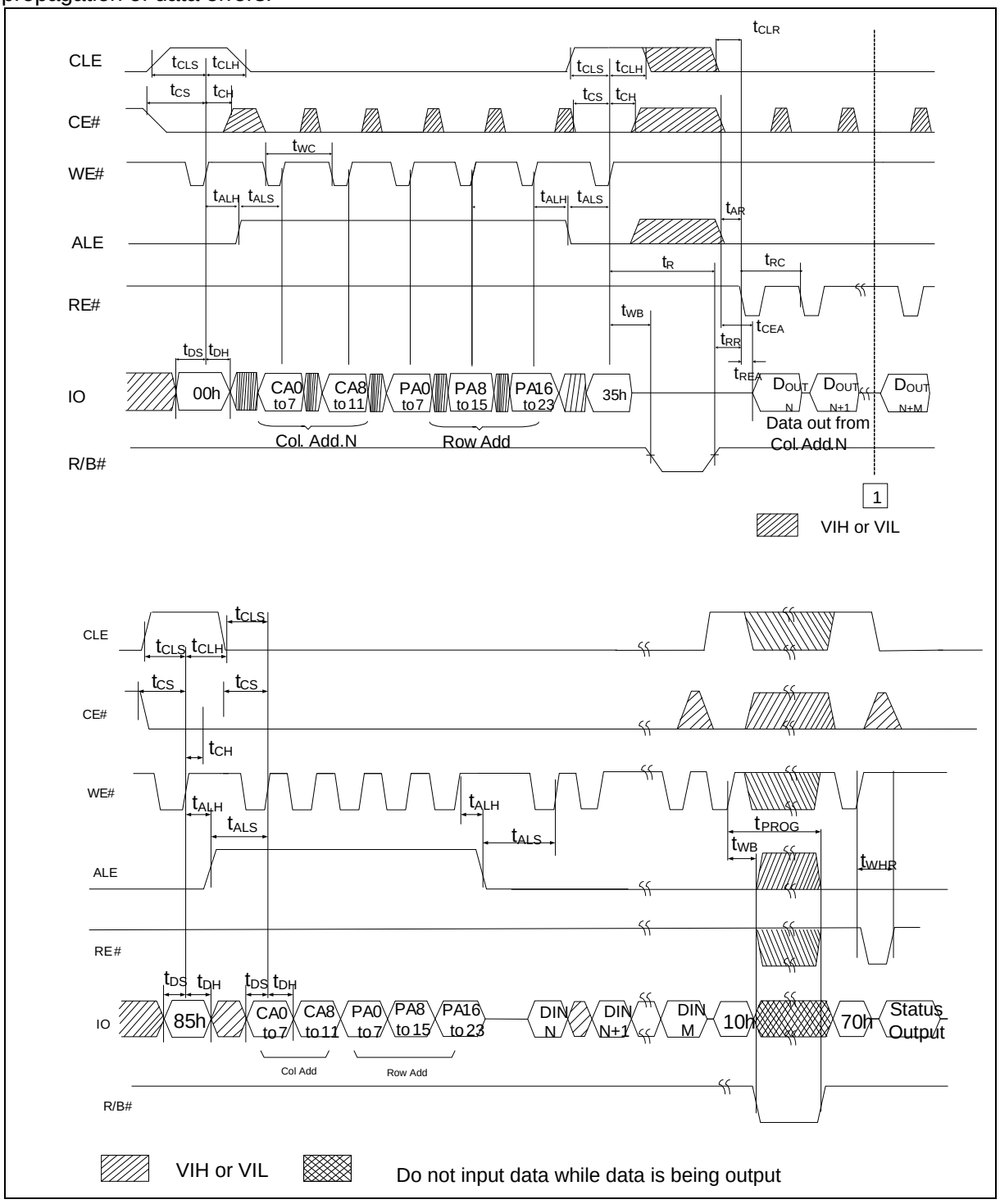


Figure 14 Copy-Back Program operation

3.2. Page Program Operation

3.2.1. Common Page Program(80h-10h)

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a word or consecutive bytes up to 4,352, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for a single page. The addressing should be done in sequential order in a block.

A page program cycle consists of a serial data loading period in which up to 4,352bytes of data may be loaded into the cache register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded.

The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the status register.

The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit(IO 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(IO 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

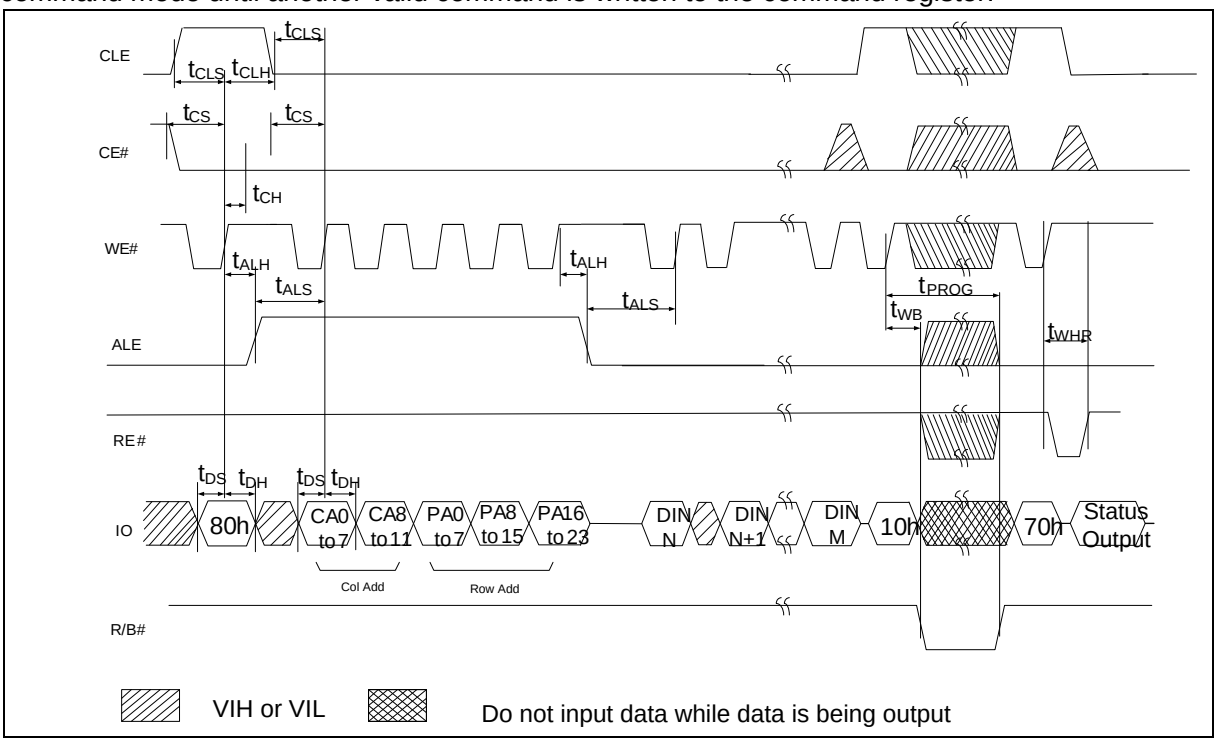


Figure 15 Program & Read Status Operation

3.2.2. Page Program Operation with Random Data Input(85h)

The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

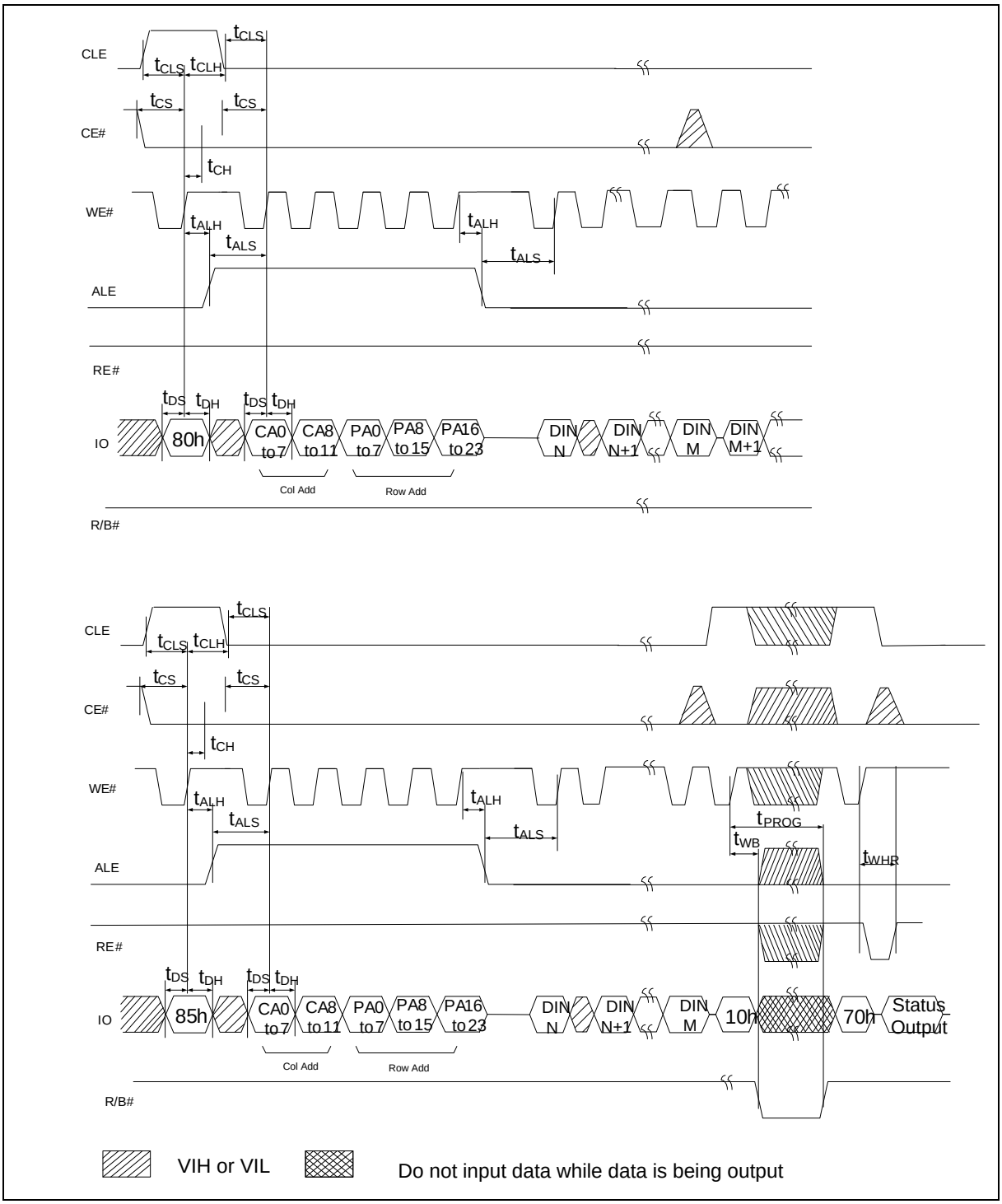


Figure 16 Random Data Input In a Page

3.2.3. Copy-Back Program with Random Data Input(85h-10h)

The Copy-Back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved.

The benefit is especially obvious when a part of a block is updated and the rest of the blocks also needs to be copied to the newly assigned free block.

The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 4,352-byte data into the internal cache register. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (85h) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed. When there is a program-failure at Copy-Back operation, error is reported by pass/fail status.

Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit(IO 6) of the Status Register.

When the Copy-Back Program is complete, the Write Status Bit(IO 0) may be checked. The internal write verification detects only errors for "1"s that are not successfully programmed to "0"s . The command register remains in Read Status command mode until another valid command is written to the command register.

During copy-back program, data modification is possible using random data input command (85h) .

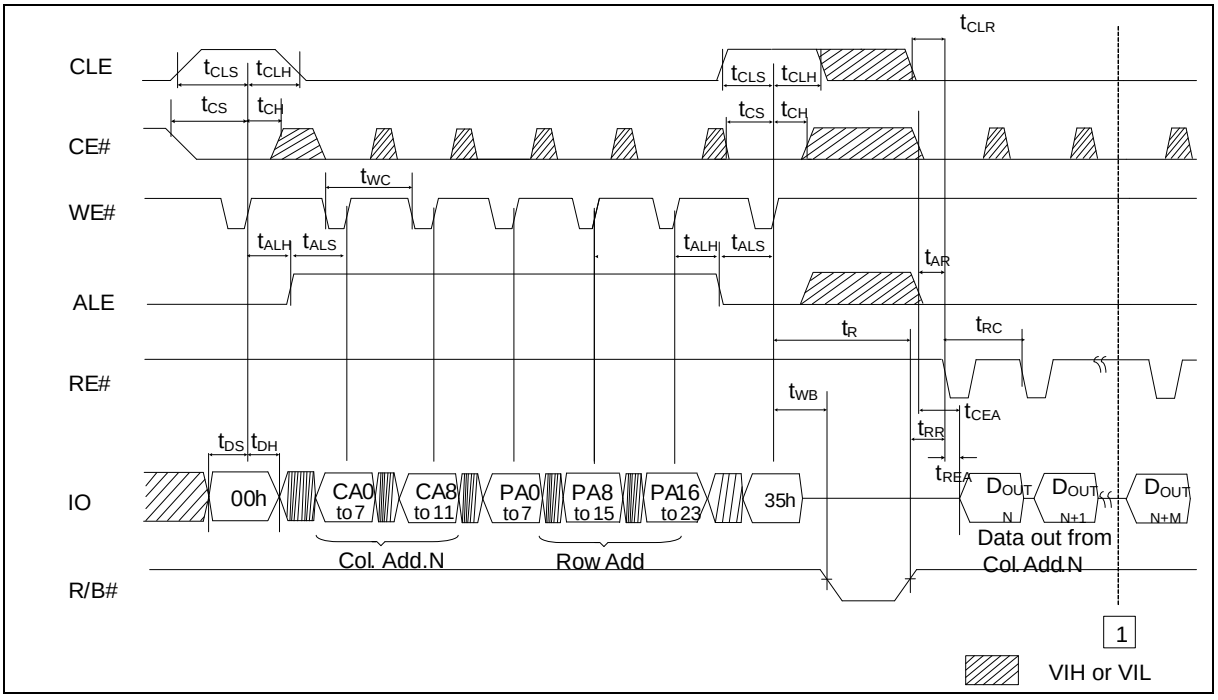


Figure 17 Page Copy-Back Program Operation

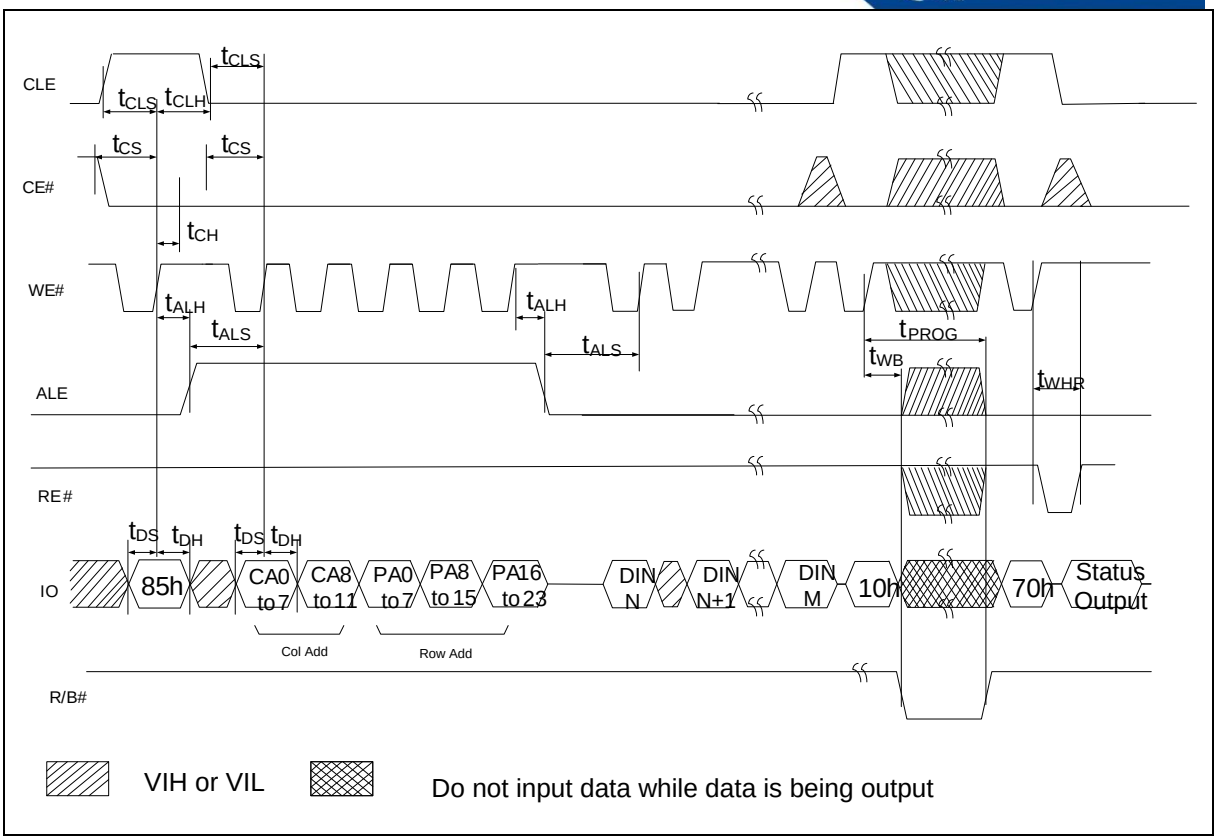


Figure 18 Page Copy-Back Program Operation with random data in

3.3. Block Erase Operation

3.3.1. Common Block Erase Operation(60h-D0h)

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command (60h). Only address PA6 to PA17 is valid while PA0 to PA5 is ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/B# output, or the status bit IO6 of the Status Register. Only the Read Status command and Reset command are valid while erasing in progress. When the erase operation is completed, the Write Status Bit(IO 0) may be checked.

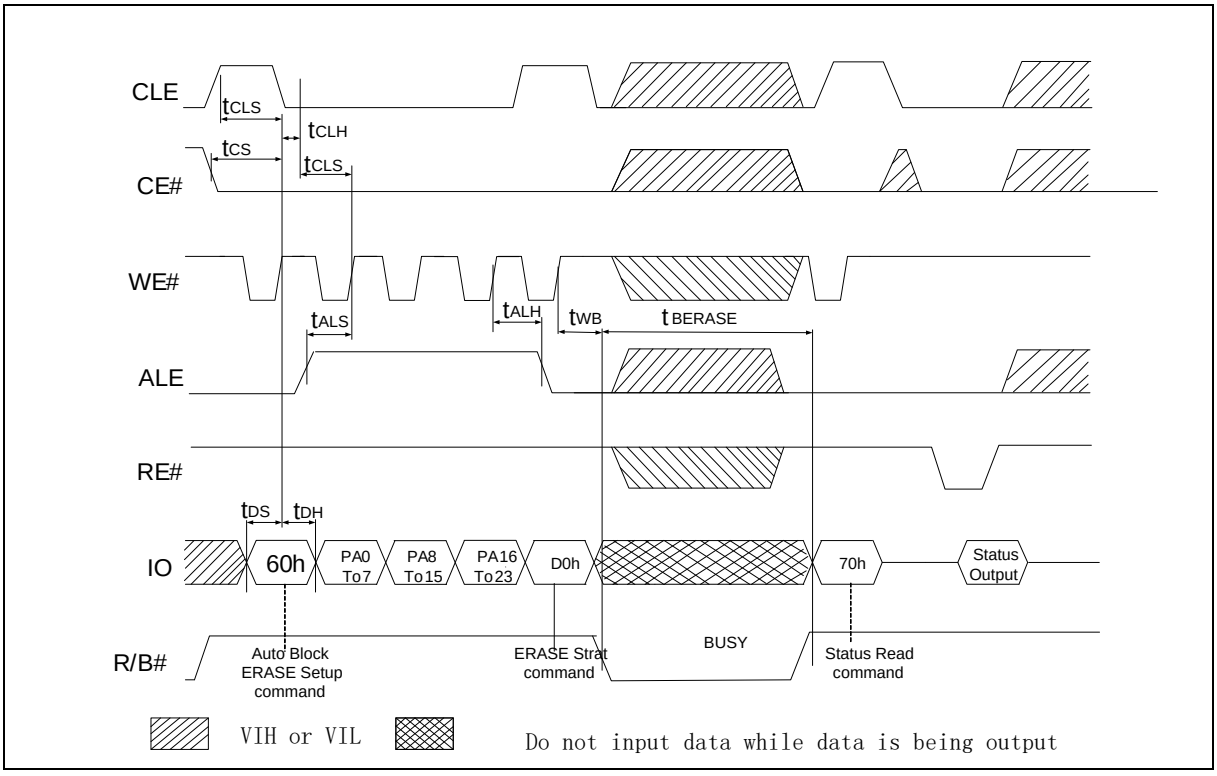


Figure 19 Block Erase Operation

3.4. Reset(FFh)

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when R/B# is high. If the device is already in ready state a new reset command will be accepted by the command register. The R/B# pin changes to low for t_{RST} after the Reset command is written.

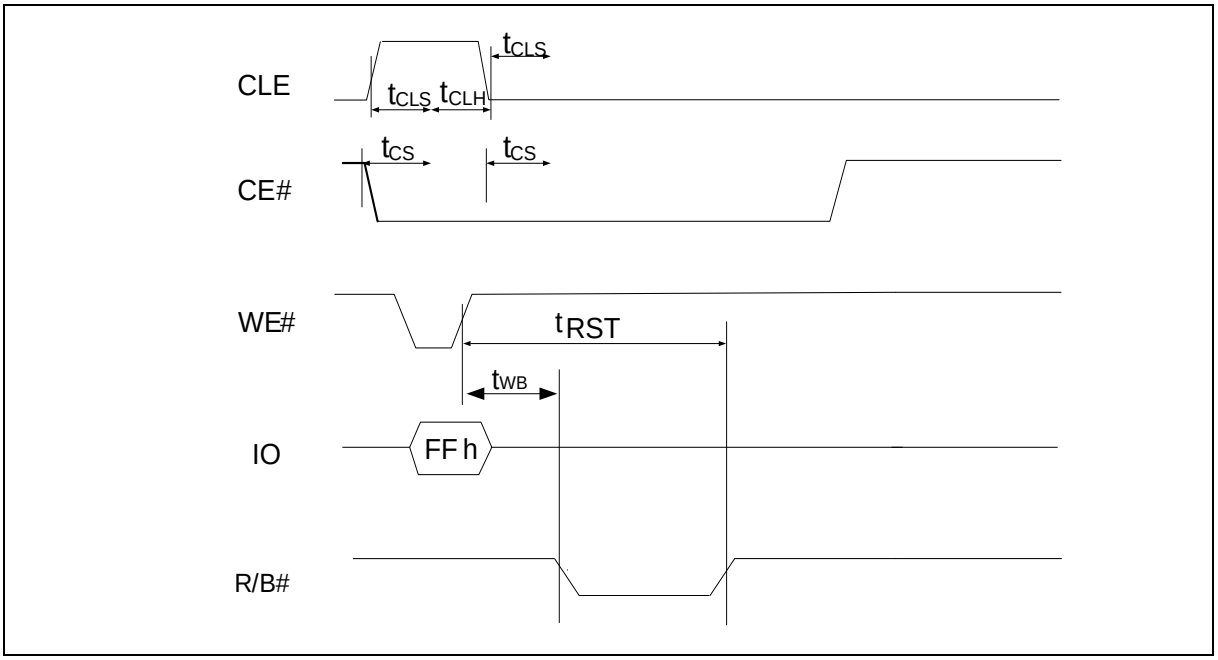


Figure 20 Reset Operation

3.5. Read Device information

3.5.1. Read ID and ONFI Signature (90h)

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (A1h), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.Figure 21 shows the operation sequence.

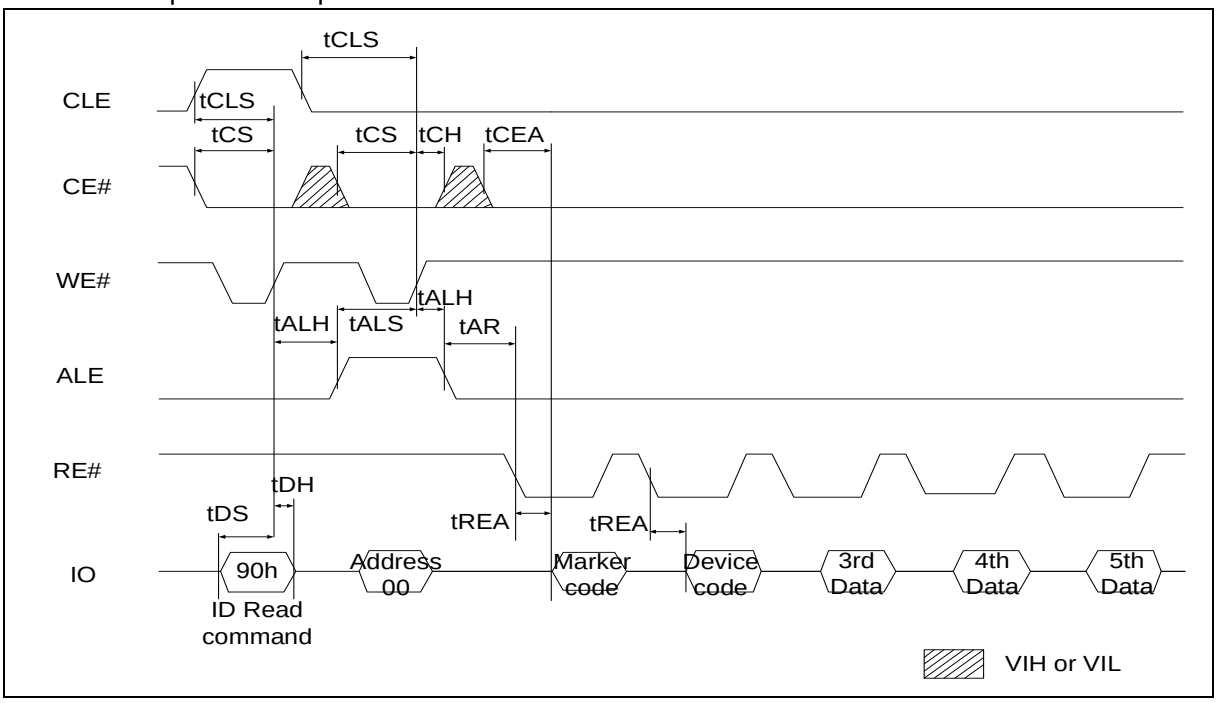


Figure 21 Read ID Operation

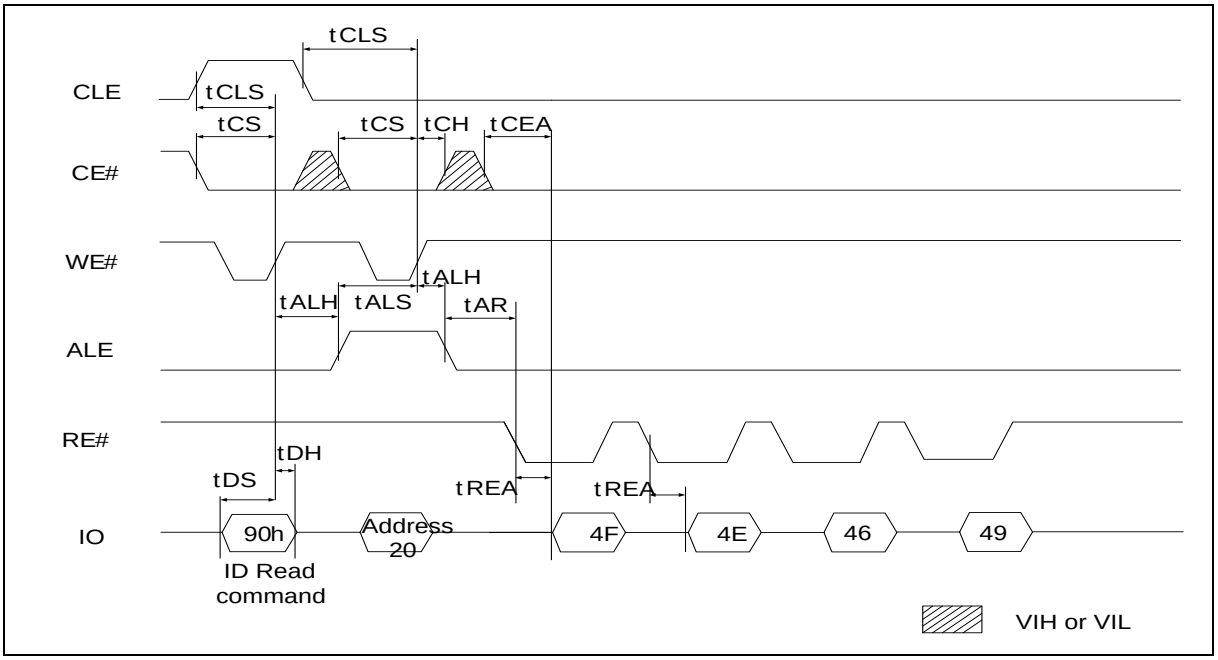


Figure 22 Read Signature

Device	Maker Code	Device Code	3rd Cycle	4th Cycle	5th Cycle
FM29F08I3	A1h	F4h	01h	26h	67h
FM29LF08I3	A1h	A4h	01h	26h	67h

Read ID Definition Table

3rd ID Data

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleave Program Between multiple chips	Not support		0						
	Support		1						
Cache program	Not Support	0							
	Support	1							

4rd ID Data

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Page Size (w/o redundant area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Block Size (w/o redundant area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Spare Area Size (byte/512 Byte)	16						0		
	32						1		
IO Organization	X8		0						
	X16		1						
Serial Access Minimum	45ns/30ns	0				0			
	20ns	1				0			
	Reserved	0				1			
	Reserved	1				1			

5rd ID Data

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size(w/o redundant Area)	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
ECC Level	1 bit/512 Byte							0	1
	2 bit/512 Byte							1	0
	4 bit/512 Byte							0	0
	8 bit/512 Byte							1	1
Internal ECC	ECC disable	0							
	ECC enable	1							

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered. The ONFI signature is the ASCII encoding of ‘ONFI’ where ‘O’ = 4Fh, ‘N’ = 4Eh, ‘F’ = 46h, and ‘I’ = 49h. Reading beyond four bytes yields indeterminate values. Figure 22 shows the operation sequence.

3.5.2. Read Unique ID(EDh)

The Read Unique ID function is used to retrieve the 16 byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement shall be stored by the target. For example, reading bytes 32-63 returns to the host another copy of the UID and its complement.

To change the data output location, it is recommended to use the Random Data Out command set (05H-E0H).The Status Read command (70H) can be used to check the completion. To continue the read operation, a following read command (00h) to re-enable the data out is necessary.

Bytes	Value
0-15	UID
16-31	UID complement(bit-wise)

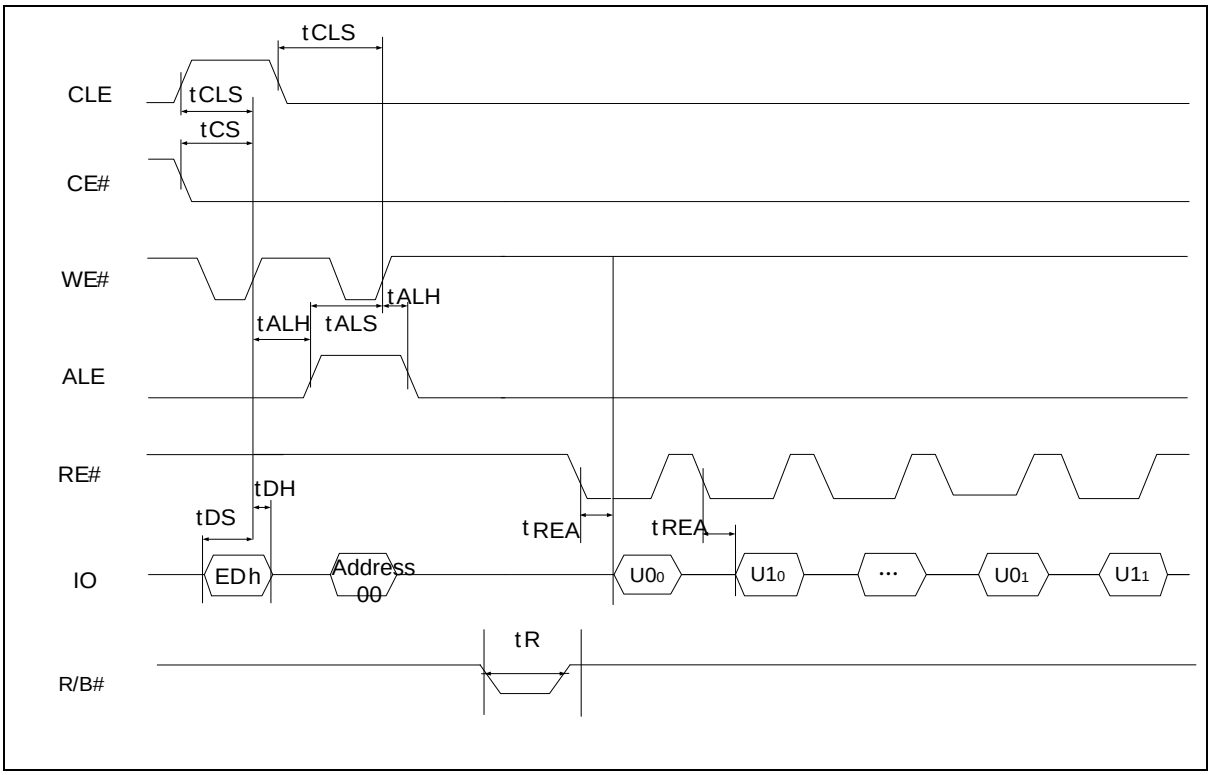


Figure 23 Read Unique ID Operation

3.5.3. Read Parameter Page (ECh)

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing and other behavioral parameters. This data structure enables the host processor to automatically recognize the NAND Flash configuration of a device. A minimum of three copies of the parameter page are stored in the device. The Read Status command (70H) may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00H is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

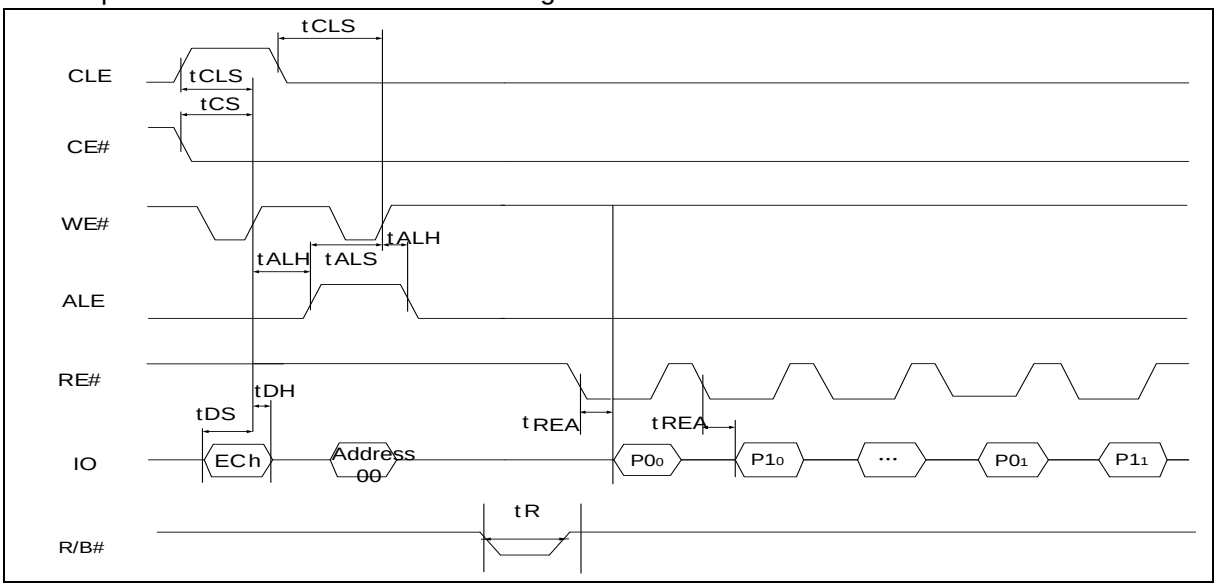


Figure 24 Read Parameter ID Operation

Byte Number	O/M	Descriptions	Values
0~3	M	Parameter Page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4~5	M	Revision number 2-15 Reserved(0) 1 1=supports ONFI version 1.0 0 reserved (0)	02h,00h
6~7	M	Feature supported 6-15 reserved (0) 5 1 = supports source synchronous 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	10h,00h

Byte Number	O/M	Descriptions		Values
8~9	M	Optional command supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command		3bh,00h
10~31		Reserved		All 00h
32~43	M	Device manufacture (12 ASCII characters)“FUDANMICRO ”		46h,55h,44h,41h, 4eh,4dh,49h,43h, 52h,4fh, 20h, 20h
44~63	M	Device model (20 ASCII characters)	“FM29F08I3”	46h,4dh,32h,39h, 46h,30h,38h, 49h, 33h,20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h,20h
			“FM29LF08I3”	46h,4dh,32h,39h, 4Ch,46h,30h, 38h, 49h,33h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h,20h
64	M	Manufacture ID		A1h
65~66	O	Date code		00h,00h
67~79		Reserved		All 00h
80~83	M	Number of data bytes per page		00h, 10h, 00h, 00h
84~85	M	Number of spare bytes per page		00h, 01h
86~89	M	Number of data bytes per partial page		00h, 02h, 00h, 00h
90~91	M	Number of spare bytes per partial page		20h,00h
92~95	M	Number of pages per block		40h, 00h, 00h, 00h
96~99	M	Number of blocks per block unit		00h, 08h, 00h, 00h
100	M	Number of logic units		02h
101	M	Number of address bytes		23h
102	M	Number of bits per cell		01h
103~104	M	Bad blocks maximum per LUN		28h, 00h
105~106	M	Block endurance		0Ah,04h
107	M	Guaranteed valid blocks at beginning of target		01h
108~109	M	Block endurance for guaranteed valid blocks		01h,03h
110	M	Number of programs per page		04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved		00h

Byte Number	O/M	Descriptions	Values
		0 1 = partial page programming has constraints	
112	M	Number of ECC bits	08h
113	M	Interleaved addressing 4-7 Reserved (0) 0-3 Number of interleaved address bits	00h
114	O	Interleaved operation attribute 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00h
115~127		Reserved	All 00h
128	M	I/O pin capacitance, maximum	0Ah
129~130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	1Fh,00h(3.3V) 0Fh,00h(1.8V)
131~132	O	Program cache timing	00H
133~134	M	Maximum page program time (μs)	84h,03h
135~136	M	Maximum block erase time (μs)	10h,27h
137~138	M	Maximum page read time (μs)	1Eh,00h
139~163		Reserved	All 00h
164~165	M	Vendor specified revision number	00h,00h
166~253		Vendor specific	All 00h
254~255	M	Integrity CRC	Set at test
256~511	M	Value of bytes 0~255	
512~767	M	Value of bytes 0~255	
768+	O	Reserved	

Notes:

1. “O” Stands for Optional, “M” for Mandatory

2. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details.

The CRC shall be calculated using the following 16-bit generator polynomial: $G(X) = X^{16} + X^{15} + X^2 + 1$

Part Number	Organization	Vcc range	CRC value Byte254-255
FM29F08I3	X8	2.7 - 3.6V	13H、84H
FM29LF08I3	X8	1.7 - 1.9V	3DH、7CH

3.6. Read Status(70h)

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to be toggled for updated status. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

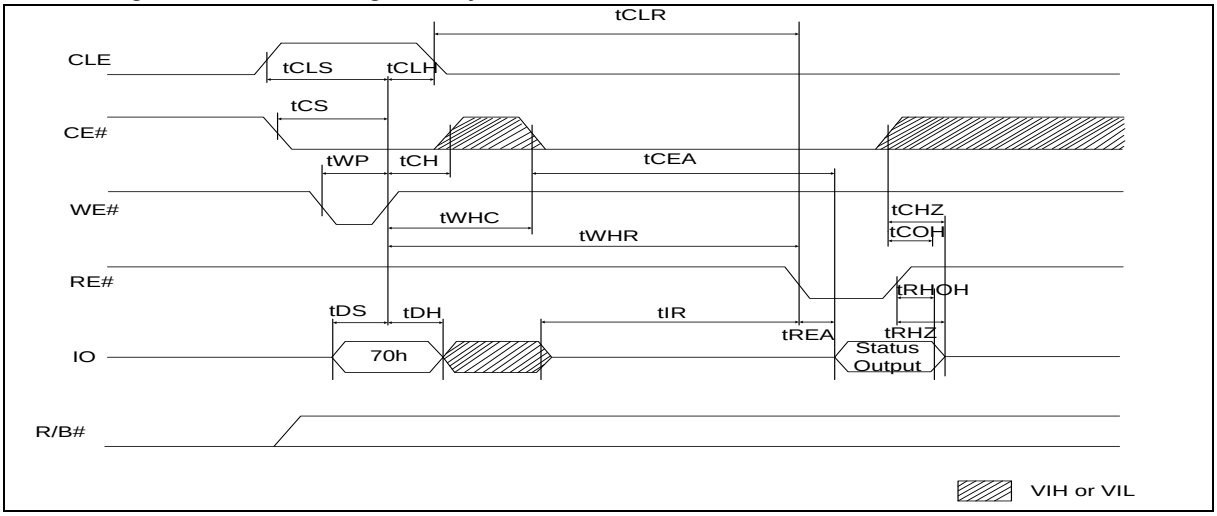


Figure 25 Status Read timing

I/O	Page Program	Block Erase	Page Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Not use	FAIL Pass：0 Fail: 1
I/O 1	Not use	Not use	Not use	FAILC Pass：0 Fail: 1
I/O 2	Not use	Not use	Not use	Not use
I/O 3	Not use	Not use	Not use	Don't Care
I/O 4	Not use	Not use	Not use	Don't Care
I/O 5	Read/Busy	Read/Busy	Read/Busy	Busy ：0 Ready： 1
I/O 6	Read/Busy	Read/Busy	Read/Busy	Busy ：0 Ready： 1
I/O 7	Write Protect	Write Protect	Write Protect	Protected：0 Not Protected：1

Table 2 Status Register Definition for 70h and 78h Command

Notes:

1. I/O0: This bit is only valid for Program and Erase operations.
2. I/O5: If set to high, then there is no array operation in progress. If cleared to 0, then there is a command being processed (I/O6 is cleared to low) or an array operation in progress.
3. I/O7: the bit indicates if the block is protected, which include WP# protection and other protection.

3.7. Read Status Enhanced(78h)

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the following cases:

-On a specific plane in case of multi-plane operations in the same die

-On a specific die in case of 2-die device

Follow figure defines the Read Status Enhanced behavior and timings. Writing 78h to the command register, followed by three row address cycles containing the page,block.

The command register remains in Status Read mode until further commands are issued.

Read Status Enhanced command is prohibited during the reset (FFh) command.

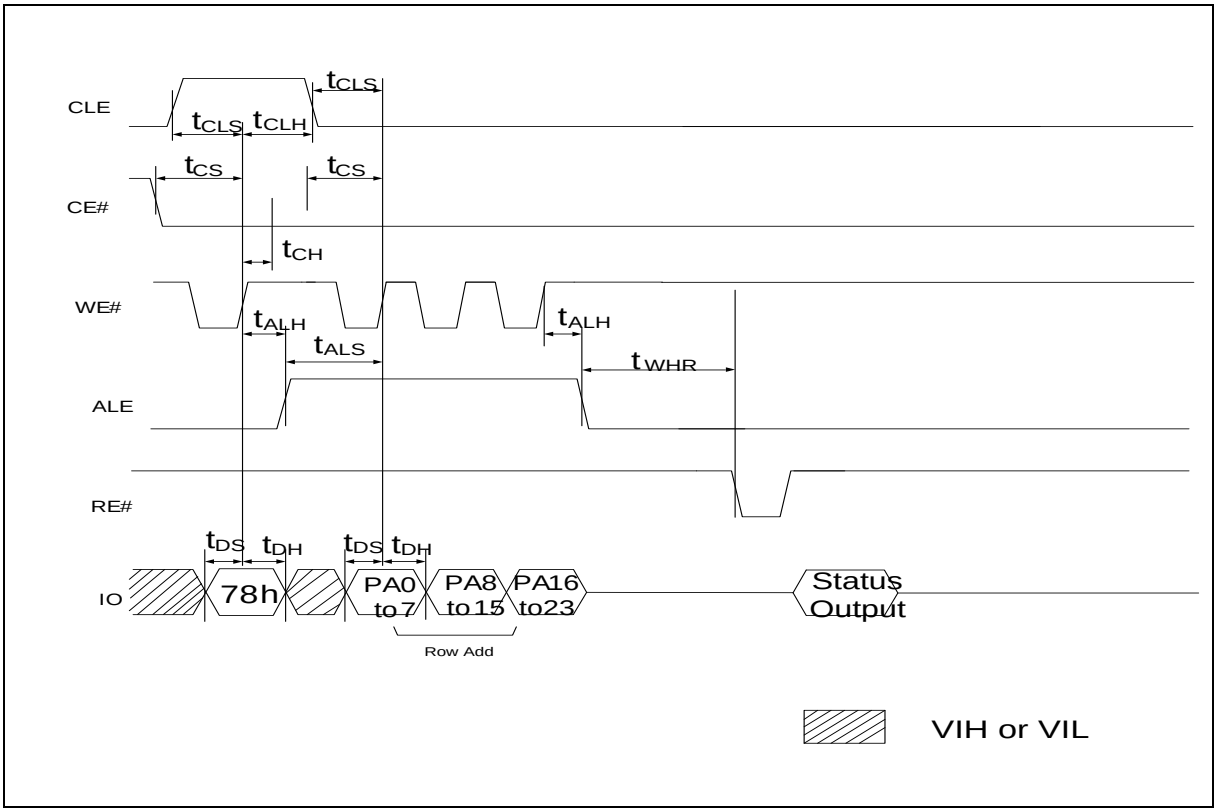


Figure 26 Status Read Enhanced timing

3.8. Ready/Busy

The device has a R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B#) and current drain during busy (ibusy) , an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.

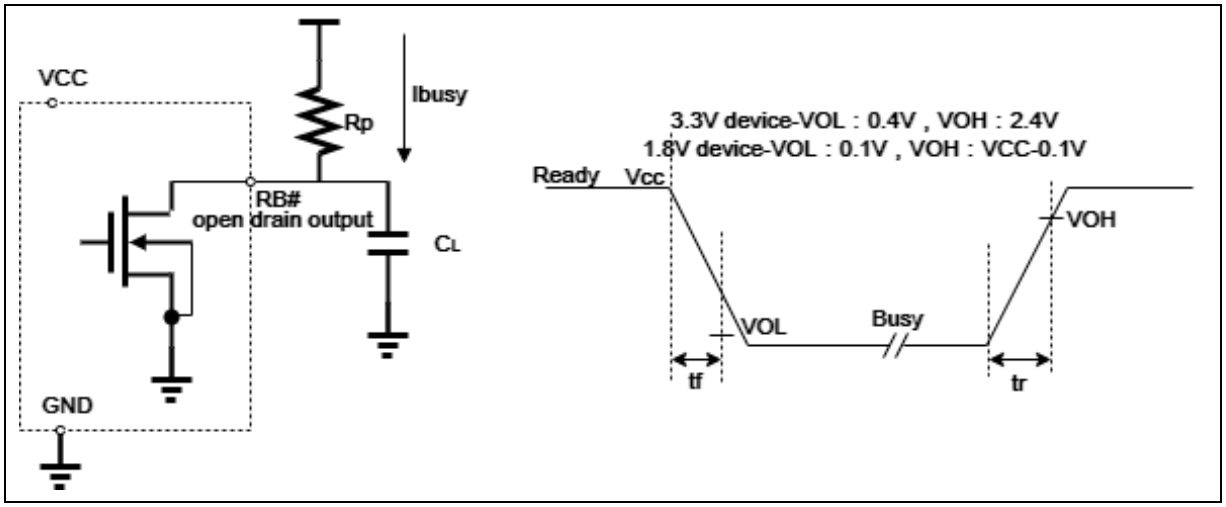
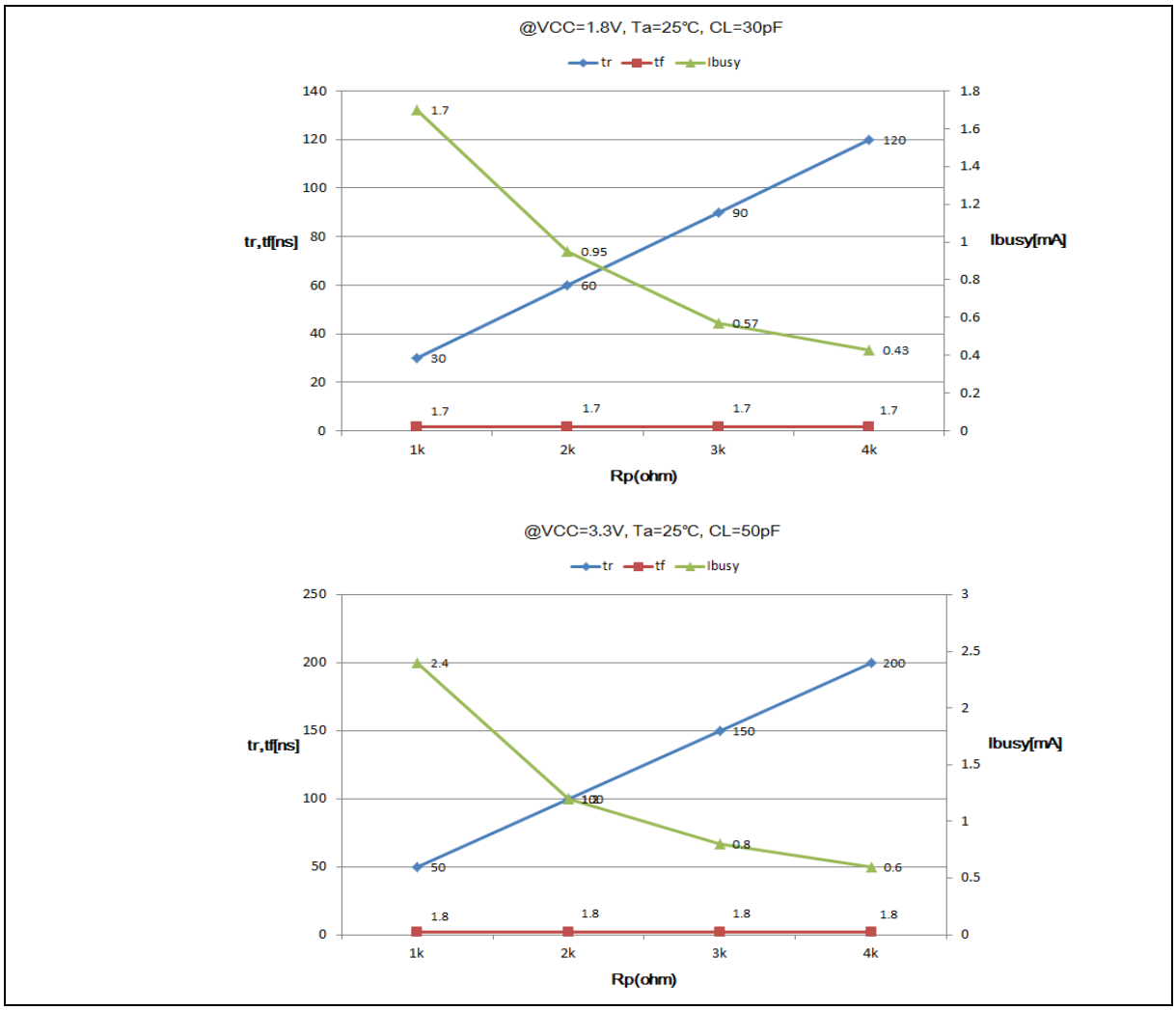


Figure 27 Rp Vs tr,tf & Rp vs ibusy



Rp value guidance

$$Rp\ (min,3.3v) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

$$Rp\ (min,1.8v) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B# pin.

Rp(max) is determined by maximum permissible limit of tr

3.9. Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about Vth. WP# pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 2ms is required before internal circuit gets ready for any command sequences as shown in Figure 28.

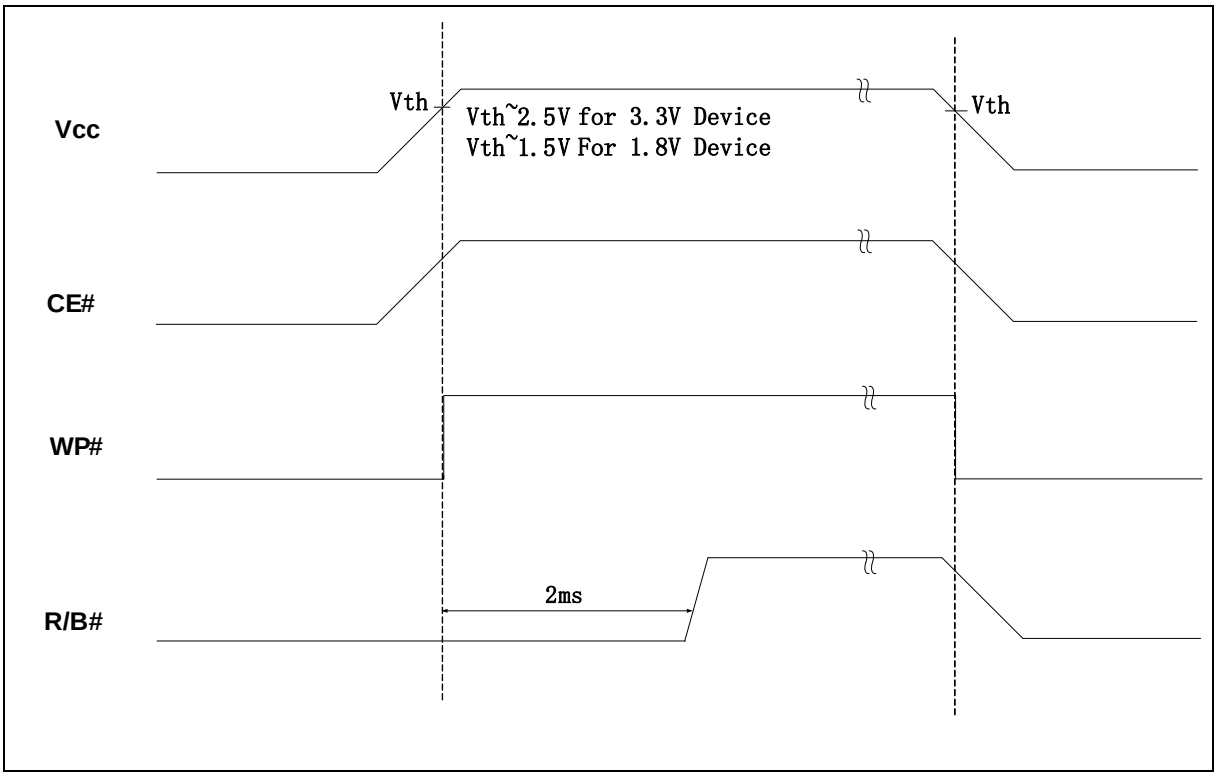


Figure 28 Data protection and power on/off

4. Electrical Characteristics

4.1. Valid Block

Parameter	Symbol	Min	Typ	Max	Unit
FM29F08I3/FM29 LF08I3	N_{VB}	4,016	—	4,096	Block

NOTE:

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 8bit/512Byte ECC.
3. Each FM29F08I3/FM29LF08I3 chip has Maximum 80 invalid blocks.

4.2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{CC}	-0.6 to Vcc+0.4	V
	V_{IN}	-0.6 to Vcc+0.4	
	$V_{I/O}$	-0.6 to Vcc+0.4	
Temperature Under Bias	T_{BIAS}	-50 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE:

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

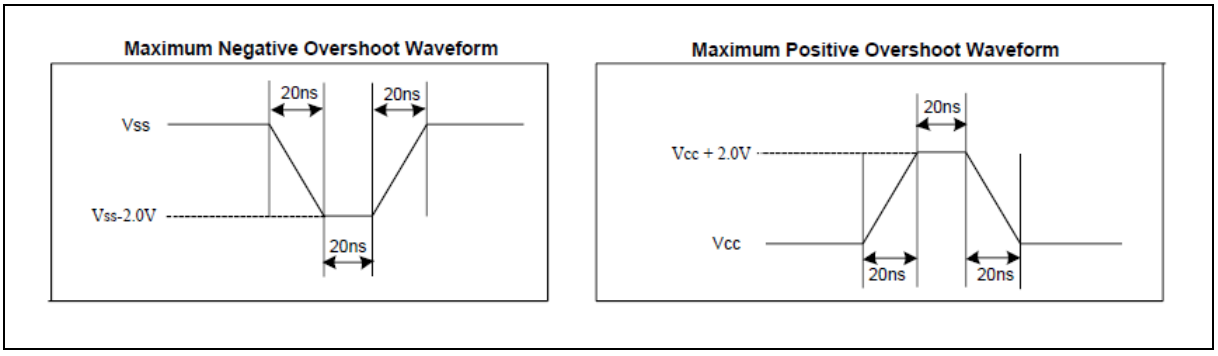


Figure 29 Input Test Waveform and Measurement Level

4.3. Recommended Operation Conditions

(Voltage reference to GND，FM29F08I3/FM29LF08I3： T_A=-40°C~85°C)

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltage	Vcc	2.7	3.3	3.6	V
1.8V Supply Voltage	Vcc	1.7	1.8	1.95	V
Supply Voltage	Vss	0	0	0	V

4.4. DC And Operating Characteristics

Parameter		Symbol	Test Conditions	3.3V			1.8V			Unit
				Min	Typ	Max	Min	Typ	Max	
Operating Current	Sequential Read	Icc1	t_{RC}=25ns,CE#=V_{IL} I_{OUT}=0mA	-	15	20	-	15	20	mA
	Program	Icc2	-							
	Erase	Icc3	-							
Standby Current(CMOS)		I_{SB2}	CE#=Vcc-0.2，WP#=0v/Vcc	-	10	50	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	-	-	±10	
Input High voltage		V_{IH}	-	0.8×Vcc	-	Vcc+0.3	0.8×Vcc	-	Vcc+0.3	V
Input Low voltage		V_{IL}	-	-0.3	-	0.2×Vcc	-0.3	-	0.2×Vcc	
Output High voltage Level		V_{OH}	I_{OH}=-100uA	-	-	-	Vcc-0.1	-	-	
			I_{OH}=-400uA	2.4	-	-	-	-	-	
Output Low voltage Level		V_{OL}	I_{OL}=100uA	-	-	-	-	-	0.1	
			I_{OL}=2.1mA	-	-	0.4	-	-	-	
Output Low Current(R/B#)		I_{OL} (R/B#)	V_{OL}=0.1V	-	-	-	3	4		mA
			V_{OL}=0.4V	8	10		-	-	-	

NOTE:

1. VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for duration of 20ns or less.

4.5. AC Test Condition

4.5.1. Test Condition

（T_A=-40~85°C）

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	<5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and CL=50pF

4.5.2. Capacitance

(TA=25°C, f=1.0MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	VIL=0V	—	20	pF
Input Capacitance	C_{IN}	VIL=0V	—	20	pF

Note: Capacitance is periodically sampled and not 100% tested.

4.5.3. Program/Erase Characteristics

Parameter	Symbol	Test Condition	Typ	Max	Unit
Program Time	t_{PROG}	—	400	900	us
Number of Partial Program Cycles	N_{OP}	—	—	4	Cycle
Block Erase Time	t_{BERS}	—	4	10	ms

NOTE:

1. Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
2. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25°C temperature.

4.5.4. AC timing Characteristics for Command/Address/Data Input

Parameter	Symbol	3.3V		1.8V		Unit
		Min	Max	Min	Max	
CLE Setup Time	t_{CLS} (1)	10	-	10	-	ns
CLE Hold Time	t_{CLH}	5	-	5	-	ns
CE# Setup Time	t_{CS}	15	-	25	-	ns
CE# Hold Time	t_{CH}	5	-	5	-	ns
WE# Pulse Width	t_{WP}	10	-	15	-	ns
ALE Setup Time	t_{ALS}	10	-	10	-	ns
ALE Hold Time	t_{ALH}	5	-	5	-	ns
Data Setup Time	t_{DS}	7	-	10	-	ns
Data Hold Time	t_{DH}	5	-	5	-	ns
Write Cycle Time	t_{WC}	20	-	30	-	ns
WE# High Hold Time	t_{WH}	7	-	10	-	ns
Address to Data Loading Timing	t_{ADL} (2)	70	-	100	-	ns

NOTE:

1. The transition of the corresponding control pins must occur only once while WE# is held low
2. t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle

4.5.5. AC Characteristics for Operation

Parameter	Symbol	3.3V		1.8V		Unit
		Min	Max	Min	Max	
Data Transfer From Cell to Register	t_R	-	30	-	40	us
ALE to RE# Delay	t_{AR}	10	-	10	-	ns
CLE to RE# Delay	t_{CLR}	10	-	10	-	ns
Ready to RE# Low	t_{RR}	20	-	20	-	ns
RE# Pulse Width	t_{RP}	10	-	15	-	ns
WE# High to Busy	t_{WB}	-	100	-	100	ns
Read Cycle Time	t_{RC}	20	-	30	-	ns
RE# Access Time	t_{REA}	-	20	-	30	ns
CE# Access Time	t_{CEA}	-	25	-	45	ns
RE# High to Output Hi-Z	t_{RHZ}	-	100	-	100	ns
CE# High to Output Hi-Z	t_{CHZ}	-	30	-	30	ns
CE# High to ALE or CLE Don't care	t_{CSD}	10		10		ns
RE# High to Output Hold	t_{RHOH}	15	-	15	-	ns
RE# Low to Output Hold	t_{RLOH}	5	-	5	-	ns
CE# High to Output Hold	t_{COH}	15	-	15	-	ns
RE# High time	t_{REH}	7	-	10	-	ns
Output Hi-Z to RE# Low	t_{IR}	0	-	0	-	ns
RE# High to WE# Low	t_{RHW}	100	-	100	-	ns
WE# High to RE# Low	t_{WHR}	60	-	60	-	ns
Device Reset Time (Read/Program/Erase)	$t_{RST}^{(1)}$	-	5/10/500	-	5/10/500	us
Write protection time	t_{WW}	100		100		ns

NOTE:

1. If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 7μs.

5. Ordering Information

FM 29F 08I3 -XXX -C -H M

Company Prefix

FM = Fudan Microelectronics Group Co.,ltd

Product Family

29F = 3.3V PPI NAND Flash

Product Density&Version

08 = 8G-bit (Page Size 4K+256 bytes)
I3= Operating Range -40℃ ~+85℃

Package Type

TP = TSOP48 (12x20mm)
BGA = BGA63 (9x11mm)

Product Carrier

A = Tray

HSF ID Code

G = RoHS Compliant, Halogen-free, Antimony-free

MSL Level

3= MSL3

FM 29LF 08I3 -XXX -C -H M

Company Prefix

FM = Fudan Microelectronics Group Co.,ltd

Product Family

29LF = 1.8V PPI NAND Flash

Product Density&Version

08 = 8G-bit (Page Size 4K+256 bytes)
I3= Operating Range -40℃ ~+85℃

Package Type

TP = TSOP48 (12x20mm)
BGA = BGA63 (9x11mm)

Product Carrier

A = Tray

HSF ID Code

G = RoHS Compliant, Halogen-free, Antimony-free

MSL Level

3= MSL3

6. Part Marking Scheme

TSOP48 12x20mm

Moisture Sensitivity Level
Blank=MSL3

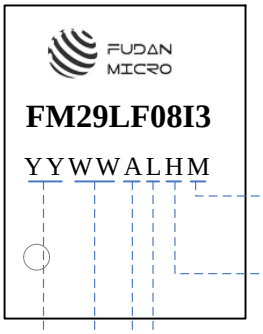
HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the product was molded (eg..week 12)

The last two digits of the year In which the product was sealed / molded.



Moisture Sensitivity Level
Blank=MSL3

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

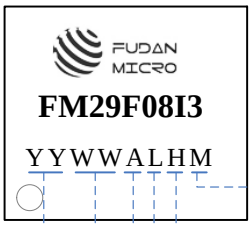
Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the product was molded (eg..week 12)

The last two digits of the year In which the product was sealed / molded.

BGA63 9x11mm



Moisture Sensitivity Level
Blank=MSL3

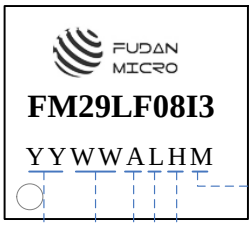
HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the product was molded (eg..week 12)

The last two digits of the year In which the product was sealed / molded.



Moisture Sensitivity Level
Blank=MSL3

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the product was molded (eg..week 12)

The last two digits of the year In which the product was sealed / molded.

7. Package Information

7.1. Pin configuration (TSOP48)

FM29F08I3/FM29LF08I3 is offered in 48-pin TSOP package as shown in Figure 30. Package diagram and dimension are illustrated in Figure 31.

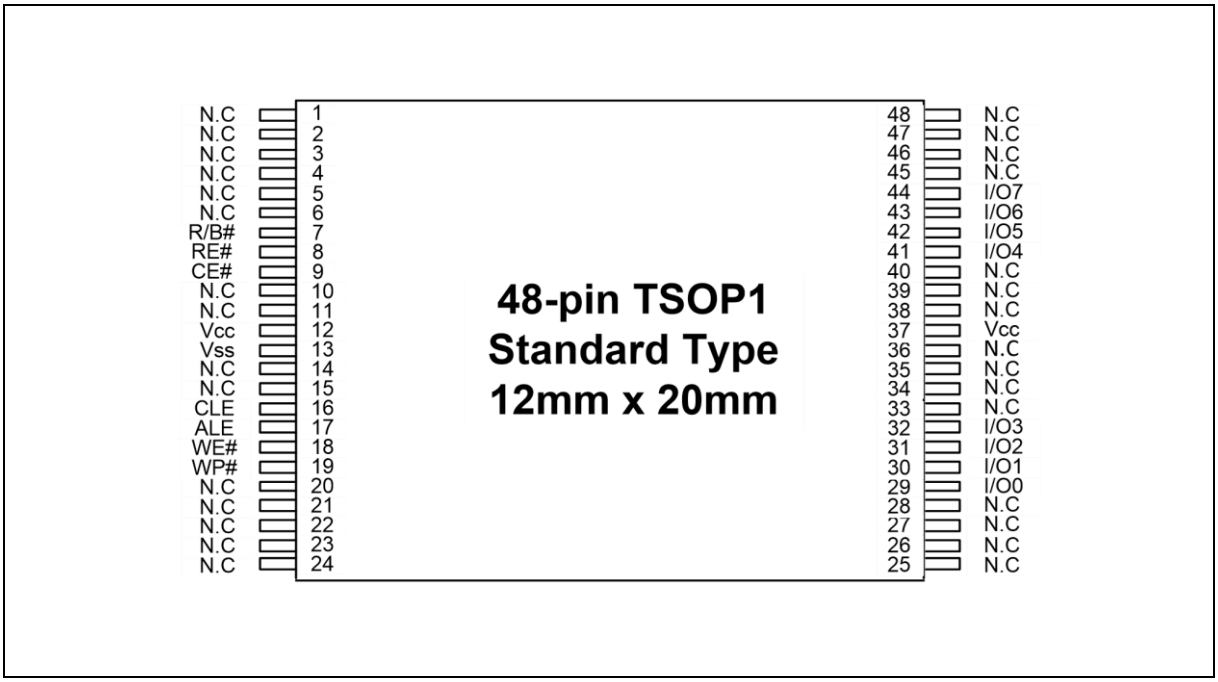
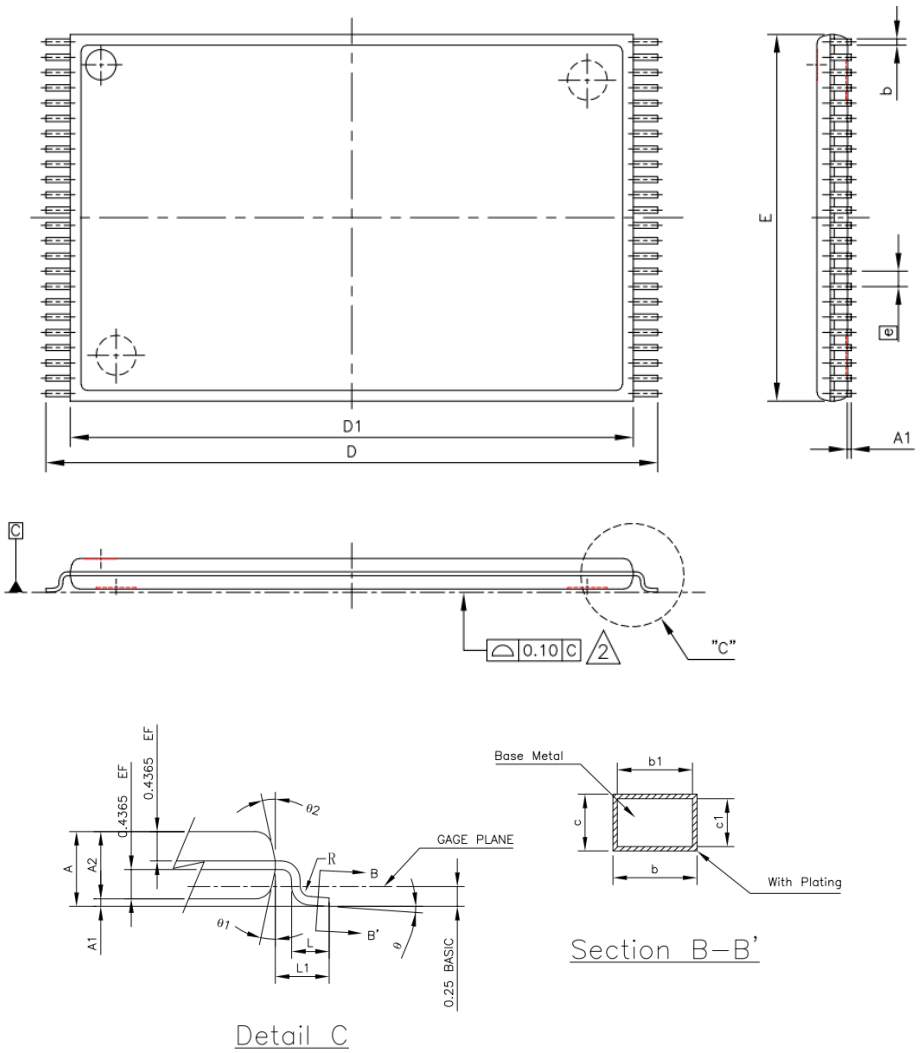


Figure 30 FM29F08I3/FM29LF08I3 pad assignments, TSOP48

7.2. Package Dimensions (TSOP48)



Symbol	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	-
A2	0.950	1.000	1.050
b	0.170	0.220	0.270
c	0.090	0.150	0.210
e	0.500(BSC)		
D	19.800	20.000	20.200
D1	18.200	18.400	18.600
E	-	-	12.400
L	0.450	0.600	0.750
θ	0°	4°	8°

NOTE:Dimensions are in Millimeters.

Figure 31 TSOP48 Package Dimensions

7.3. Ball Assignment: 63-Ball FBGA (Balls Down, Top View)

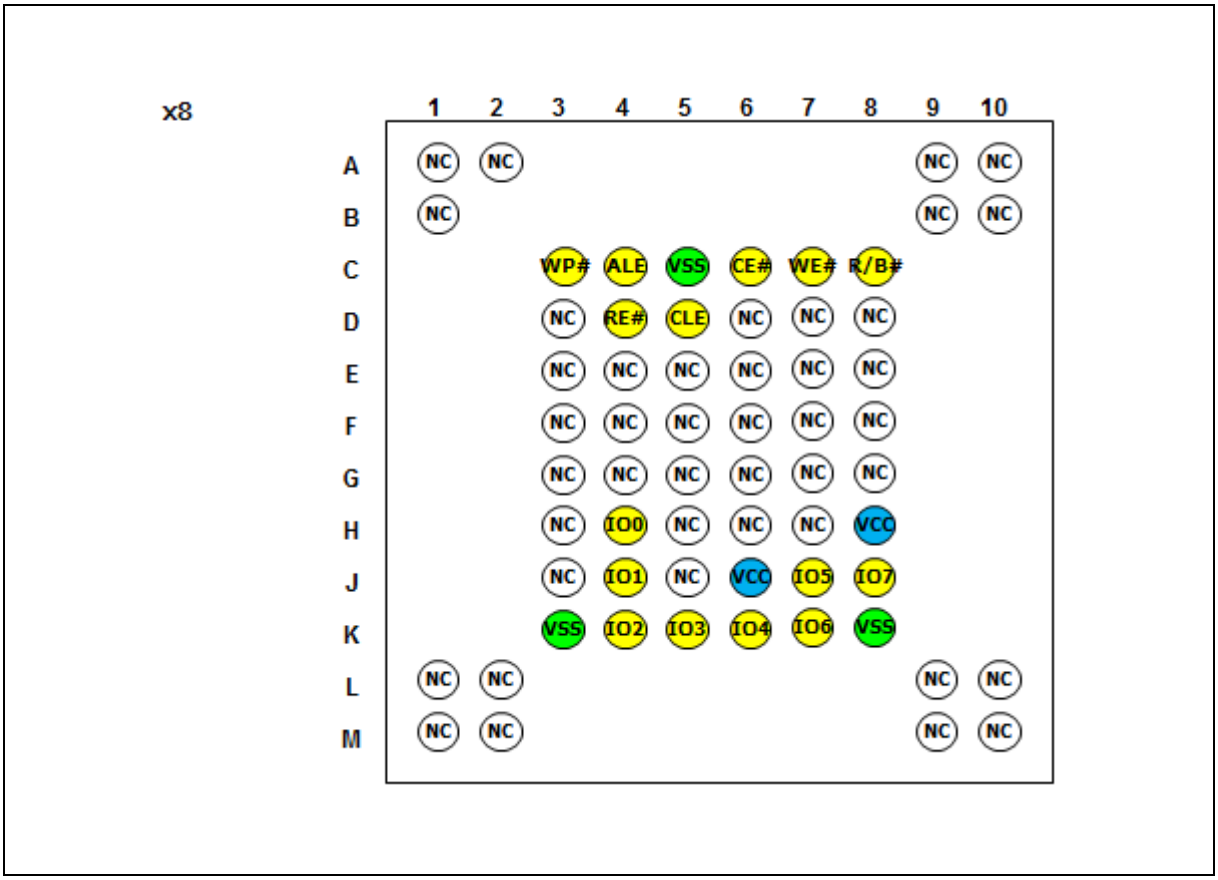
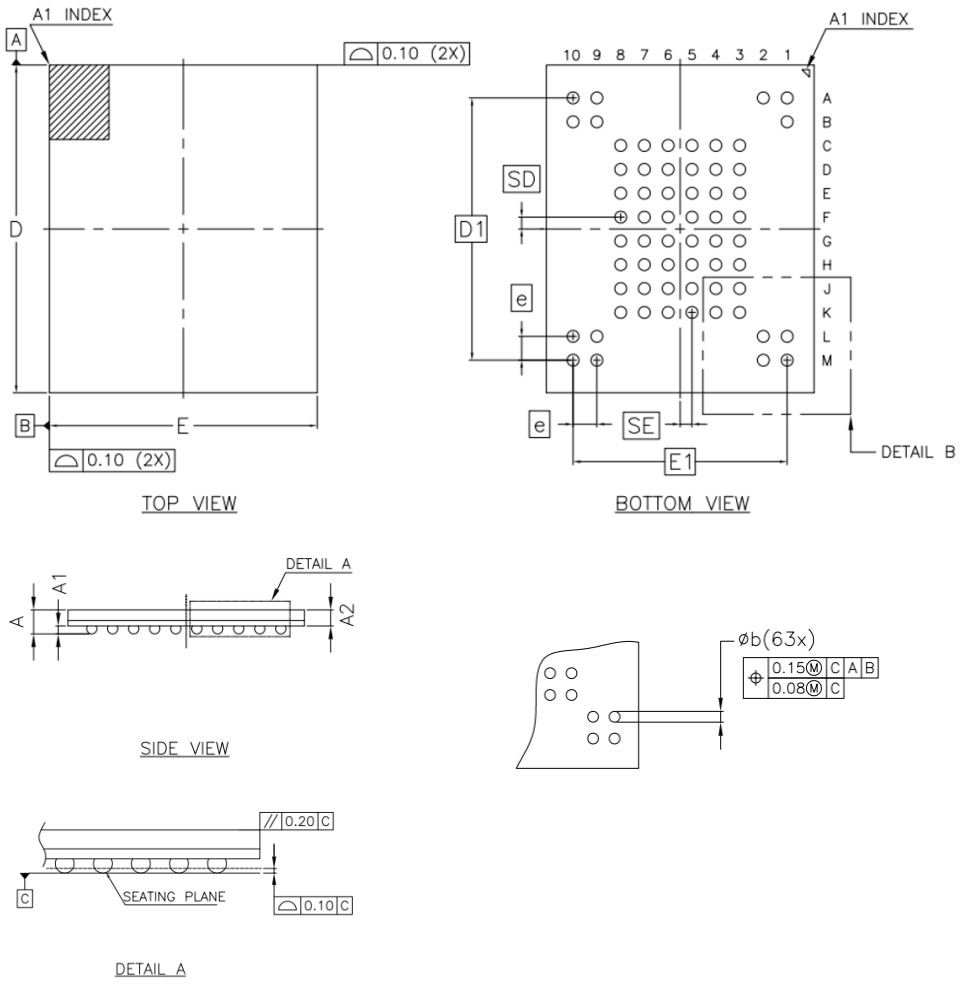


Figure 32 FM29F08I3/FM29LF08I3 ball assignments

7.4. Package Dimensions: 63-Ball FBGA (Balls Down, Top View)



Symbol	MIN	NOM	MAX
A	-	-	1.000
b	0.350	0.400	0.450
D	10.900	11.000	11.100
D1		8.800(BSC)	
E	8.900	9.000	9.100
E1		7.200(BSC)	
e		0.800(BSC)	
SE		0.400(BSC)	
SD		0.400(BSC)	

NOTE:

1. **Dimensions are in Millimeters;**
2. **The Diameter of Pre-reflow solder ball is Φ0.4mm**

Figure 33 BGA63 Package Dimensions

7.5. NAND Flash Technical Notes

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s)have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s)does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 8it/512Byte ECC.

Identifying Initial Invalid Block(s)

All device locations are erased (FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. FM29F08I3/FM29LF08I3 makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 4096. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart (Figure 34). Any intentional erasure of the original initial invalid block information is prohibited.

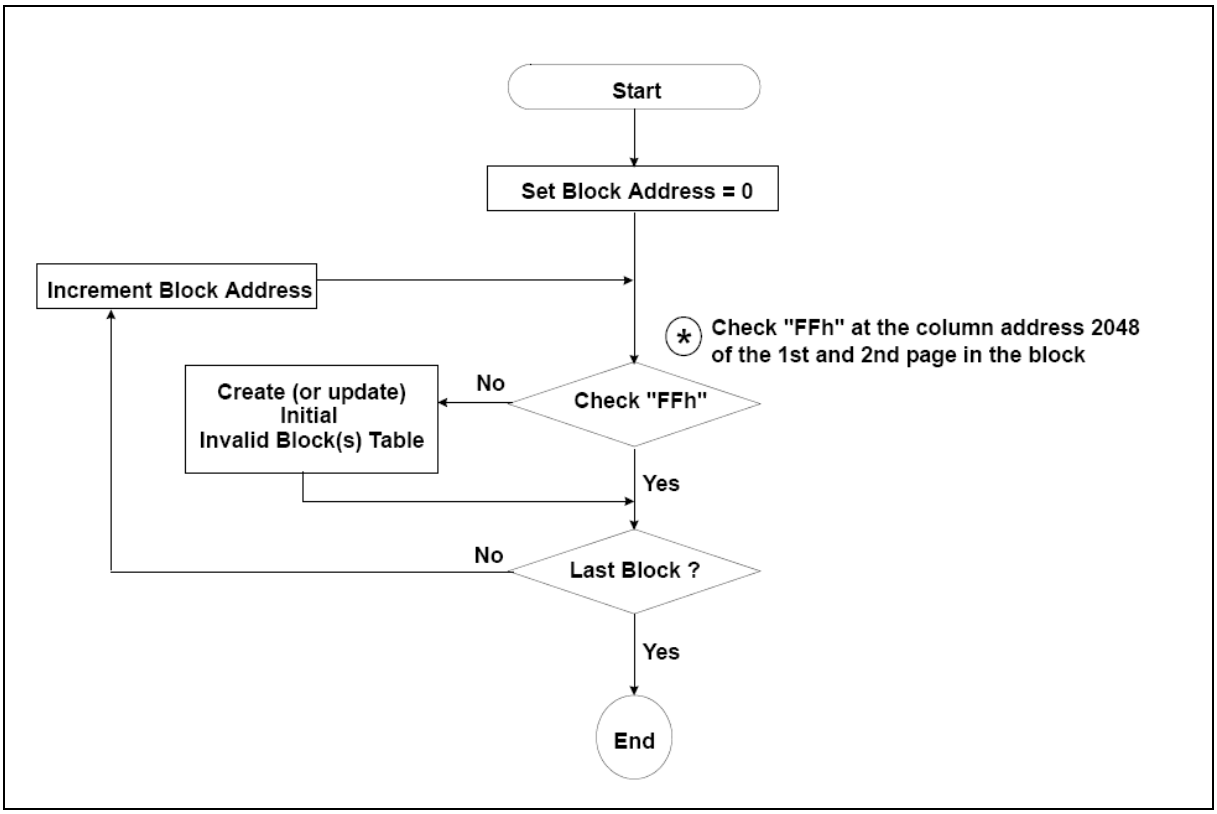


Figure 34 Flow Chart to create initial invalid block table

7.6. NAND Flash Technical Notes (Continued)

Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase-> Block Replacement
	Program Failure	Status Read after Program-> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

Program Flow Chart

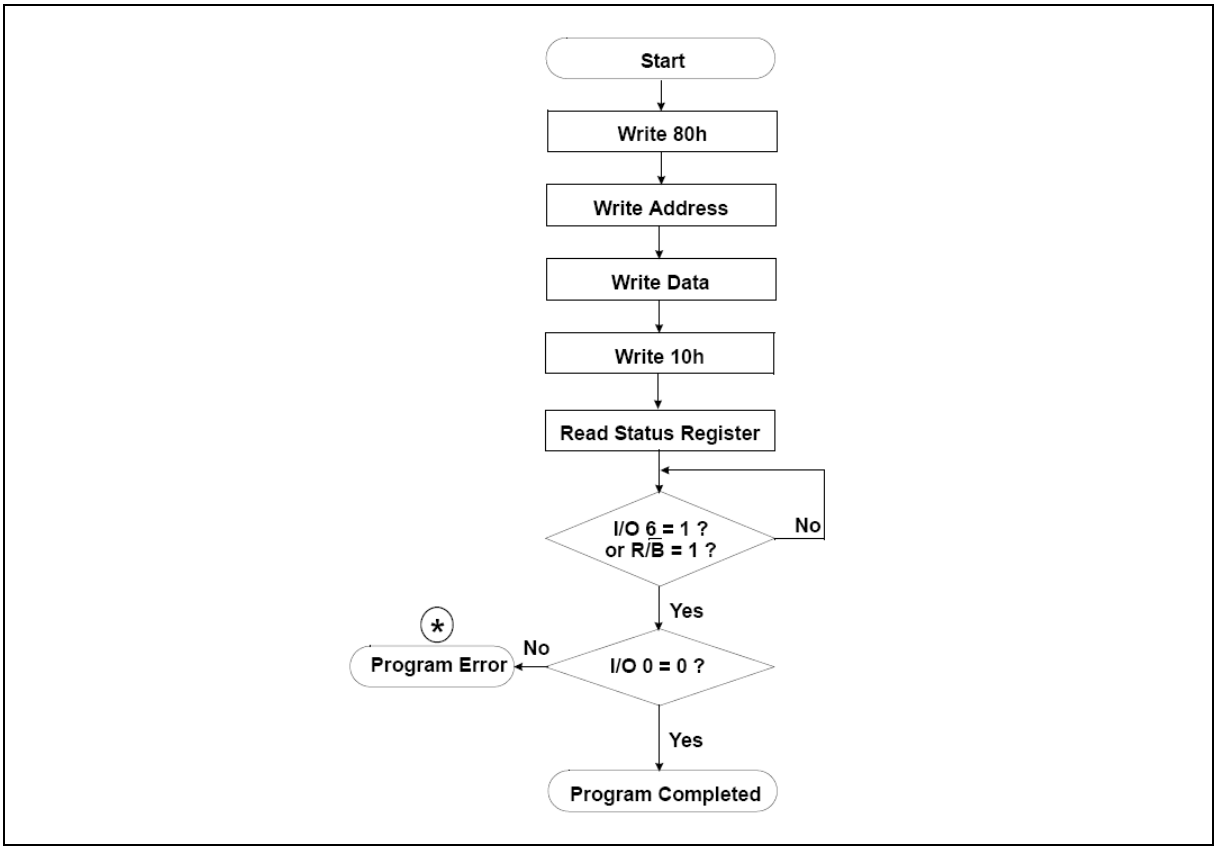
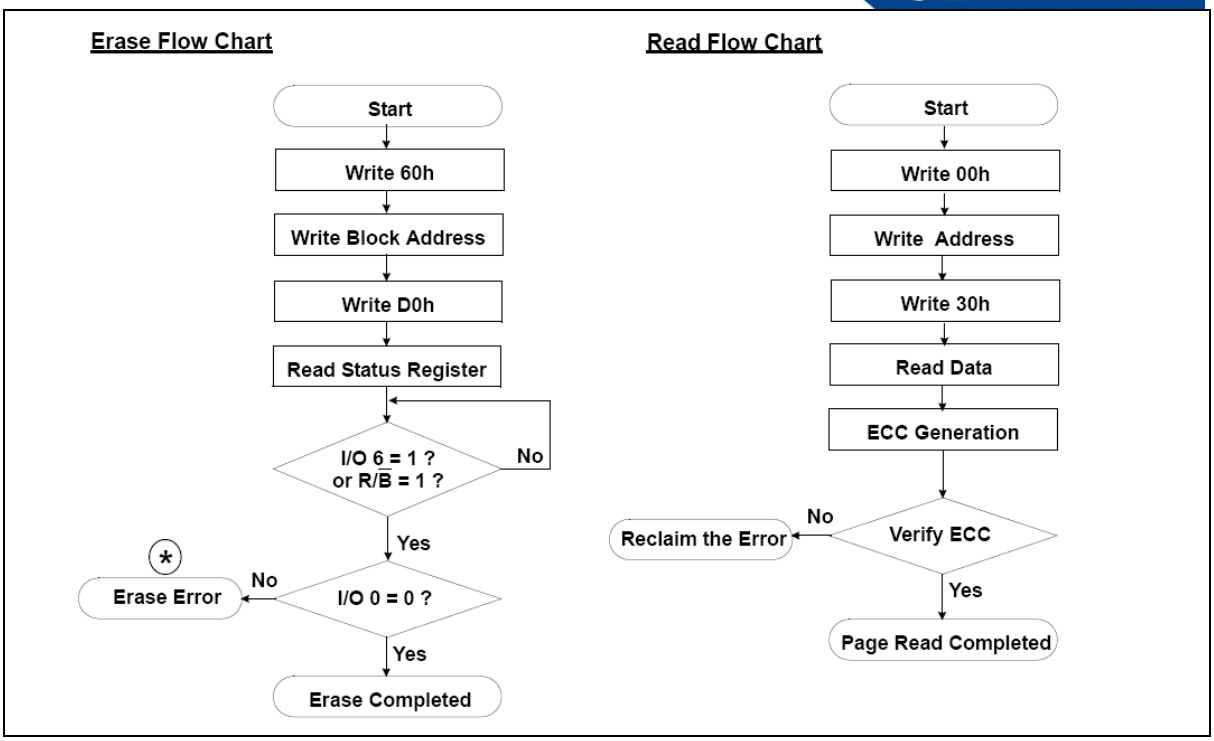


Figure 35 Program Flow Chart

* If program operation results in an error, map out the block including the page in error and copy the target data to another block.



* If erase operation results in an error, map out the failing block and replace it with another block.

Figure 36 Erase and Read Flow Chart

Block Replacement

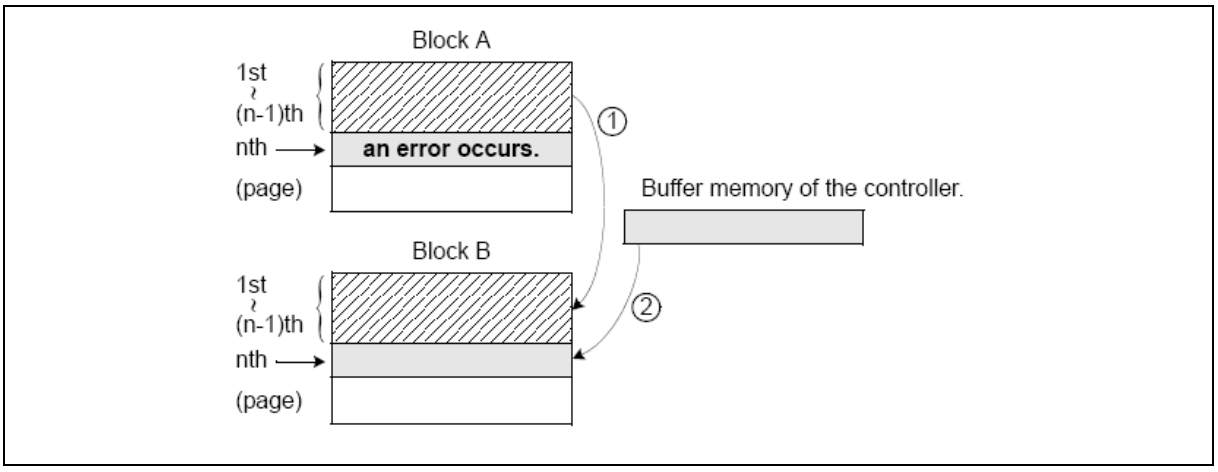


Figure 37 Block Replacement

*Step 1

When an error happens in the nth page of Block A during erase or program operation.

*Step 2

Copy the data in the 1st~(n-1)th page to the same location of another free block (Block B)

*Step 3

Then, copy the nth page data of the Block A in the buffer memory to the nth page of the Block B

*Step 4

Do not erase or program to Block A by creating an invalid block table or other appropriate scheme

Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Nov 2023	52		Initial document Release.
1.1	July 2024	52	Features 7.5	Update Endurance Program/Erase Cycles Update invalid block mark address
1.2	Aug 2024	52	3.5.3 3.8 5	Update Parameter Page Update Ready/Busy Description Update Ordering Information Description

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