FM25LQ128I3

128M-BIT SERIAL FLASH MEMORY

Datasheet

Dec.2024

1. Description

The FM25LQ128I3 is a 128M-bit (16,384K-byte) Serial Flash memory, operating in low voltage range. The FM25LQ128I3 supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O as well as 2-clock instruction cycle Quad Peripheral Interface (QPI).

The FM25LQ128I3 can be programmed 1 to 256 bytes at a time, using the Page Program instruction. It is designed to allow either single Sector/Block at a time or full chip erase operation. The FM25LQ128I3 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

2. Features

- **128Mbit of Flash memory**
  - 4096 uniform sectors with 4K-byte each
  - 256 uniform blocks with 64K-byte each or
  - 512 uniform blocks with 32K-byte each
  - 256 bytes per programmable page
- **Serial Interface**
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ0, DQ1, WP#
  - Quad SPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
  - QPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
  - DTR (Double Transfer Rate) Read
  - Continuous READ mode support
  - Program / Erase Suspend and Resume support
  - Allow true XIP (execute in place) operation
- **High Performance**
  - Max FAST_READ clock frequency: 133MHz
  - Max DTR_FAST_READ clock frequency: 104MHz
  - Max READ clock frequency:80MHz
  - Typical page program time: 0.4ms
  - Typical sector erase time: 30ms
  - Typical block erase time: 150/200ms
  - Typical chip erase time: 40s
- **Supply Voltage: 1.65V to 2.0V**
- **Industrial Temperature Rage**

- **Flexible Architecture with 4KB Sectors**
  - Uniform Sector Erase(4K-bytes)
  - Uniform Block Erase(32K and 64K-bytes)
  - Program 1 to 256 bytes per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and hardware write protection
  - Top/Bottom, 4KB complement array protection
  - Power Supply Lock-Down and OTP protection
  - Individual Block/Sector array protection
  - Lockable 4X256-Byte OTP Security Register
  - Discoverable Parameters (SFDP) Register
  - 64-Bit Unique ID for each device
  - Volatile & Non-volatile Status Register Bits
- **High Reliability**
  - Endurance: 100,000 program/erase cycles
  - Data retention: 20 years
- **Green Package**
  - 8-pin SOP (208mil)
  - 8-pin VSOP (208mil)
  - 8-pad TDFN (5x6mm)
  - 24-ball BGA (8x6mm)
  - All Packages are RoHS Compliant and Halogen-free

3. Packaging Type And Pin Configurations

FM25LQ128I3 is offered in an 8-pin SOP (208mil), an 8-pin VSOP (208mil), an 8-pad TDFN (5x6mm)and a 24-ball BGA (8x6mm) packages as shown in Figure 1-3 respectively. Package diagrams and dimensions are illustrated at the end of this datasheet.

3.1. Pin Configuration SOP8(208mil), VSOP8(208mil)

Top View

CS#	1 ○	8	VCC
DO(DQ$_1$)	2	7	HOLD#/RESET# (DQ$_3$)
WP#(DQ$_2$)	3	6	CLK
VSS	4	5	DI(DQ$_0$)
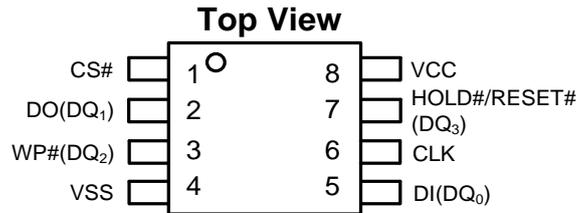
Figure 1   FM25LQ128I3 pin assignments, 8-pin SOP(208mil)

3.2. Pin Configuration TDFN8(5x6mm)

Top View

CS#	1 ○	8	VCC
DO(DQ$_1$)	2	7	HOLD#/RESET# (DQ$_3$)
WP#(DQ$_2$)	3	6	CLK
VSS	4	5	DI(DQ$_0$)
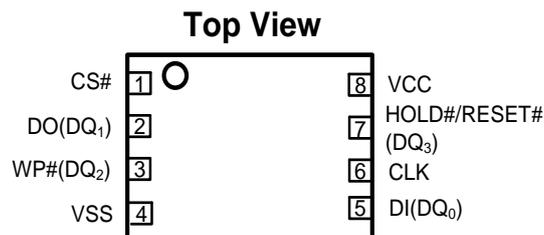
Figure 2   FM25LQ128I3 pad assignments, 8-pad TDFN(5x6mm)

3.3. Ball Configuration BGA24(8x6mm)(5x5 Ball Array)

	A2 NC	A3 NC	A4 NC	A5 NC
B1 NC	B2 CLK	B3 VSS	B4 VCC	B5 NC
C1 NC	C2 CS#	C3 NC	C4 WP#(DQ$_2$)	C5 NC
D1 NC	D2 DO(DQ$_1$)	D3 DI(DQ$_0$)	D4 HOLD#(DQ$_3$)	D5 NC
E1 NC	E2 NC	E3 NC	E4 NC	E5 NC
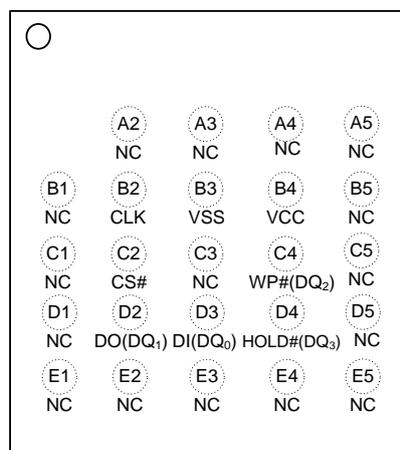
Figure 3   FM25LQ128I3 pad assignments, 24-ball BGA (8x6mm)

3.4. PinConfiguration

PIN NAME	I/O	FUNCTION
CLK	I	Serial Clock Input
VSS		Ground
VCC		Power Supply
CS#	I	Chip Select Input
WP# (DQ2)	I/O	Write Protect Input (Data Input Output 2)[2]
DO (DQ1)	I/O	Data Output (Data Input Output 1)[1]
DI (DQ0)	I/O	Data Input (Data Input Output 0)[1]
HOLD#/RESET# (DQ3)	I/O	Hold Input (Data Input Output 3)[2]
NC		No connect

Note:

1 DQ0 and DQ1 are used for Dual SPI instructions.

2 DQ0 – DQ3 are used for Quad SPI and QPI instructions

3 WP#(DQ2), HOLD#/RESET#(DQ3) will remain internal pull up function while this pin is not physically connected in system configuration. However, the internal pull up function will be disabled if the system has physical connection to WP#(DQ2) or HOLD#/RESET#(DQ3).

4. Pin Descriptions

4.1. Chip Select(CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2, DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted. The CS# input must track the VCC supply level at power-up (see "8Write Protection" and Figure 79). If needed a pull-up resister on CS# can be used to accomplish this.

4.2. Serial Data Input, Output and I/Os (DI, DO and DQ0, DQ1, DQ2, DQ3)

The FM25LQ128I3 supports standard SPI, Dual SPI, Quad SPI and QPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual/Quad SPI and QPI instructions use the bidirectional DQ pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the WP# pin becomes DQ_2 and HOLD# pin becomes DQ_3.

4.3. Write Protect(WP#)

The Write Protect (WP#) pin can be used to prevent the Status Registers from being written. The WP# pin is active low. However, when the QE bit of Status Register-2 is set for Quad I/O, the WP# pin function is not available since this pin is used for DQ2.

4.4. HOLD(HOLD#)

The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When HOLD# is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the HOLD# pin function is not available since this pin is used for DQ_3.

4.5. Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

4.6. Reset(RESET#)

The RESET# pin allows the device to be reset by the controller. For 8-pin packages, when QE=0, the DQ_3 pin can be configured either as a HOLD# pin or as a RESET# pin depending on Status Register setting.
When QE=1, the HOLD# or RESET# function is not available.

5. Block Diagram
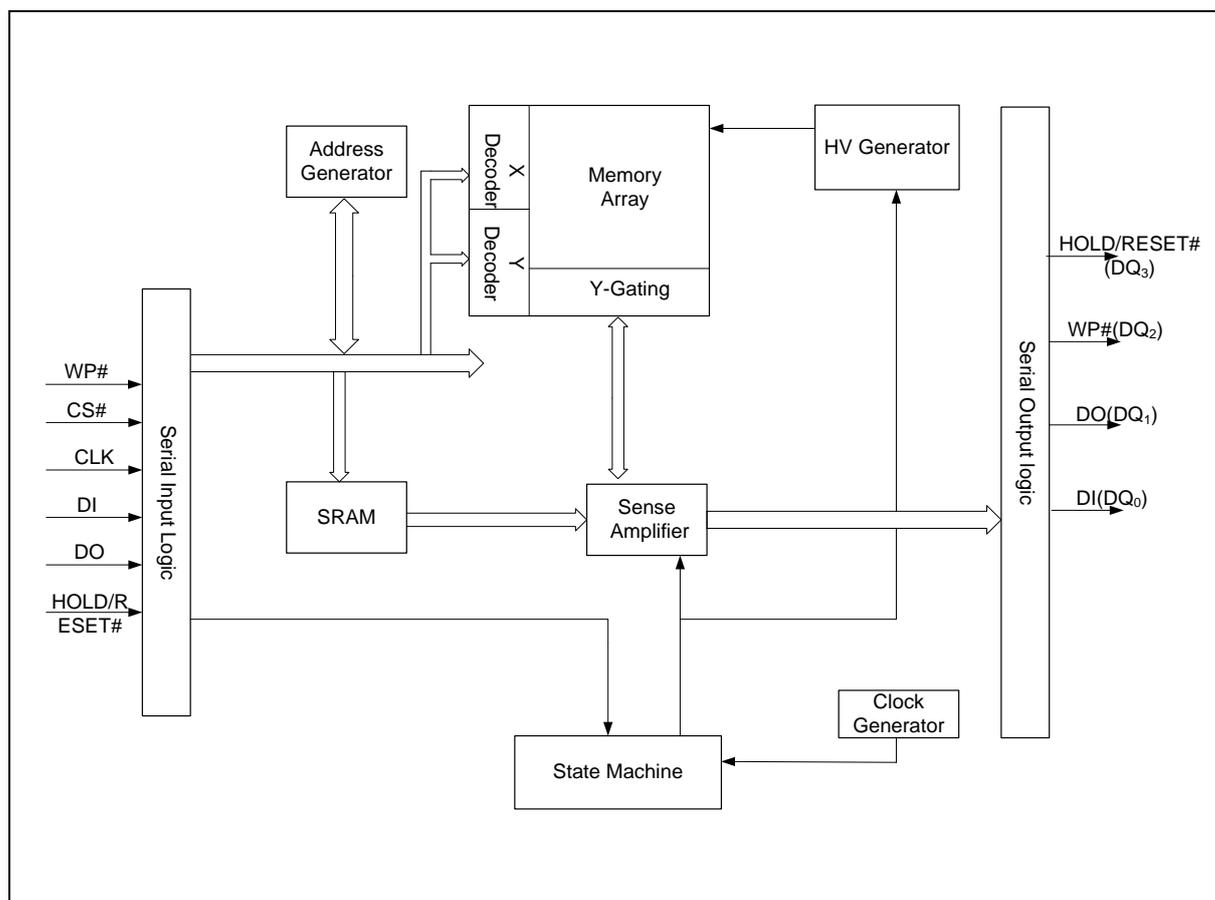
Figure 4 FM25LQ128I3 Serial Flash Memory Block Diagram

6. Memory Organization

The FM25LQ128I3 array is organized into 65,536 programmable pages of256-byteseach.Upto256bytes can be programmed (bits are programmed from 1 to 0) atatime.Pagescanbeerasedingroupsof16(4KBsectorerase),groupsof128 (32KB block erase), groups of256 (64KB block erase)ortheentirechip(chiperase).TheFM25LQ128I3 has 4,096 erasable sectors,512 erasable 32-k byte blocks and 256 erasable 64-k byte blocks respectively. The small 4KB sectorsallowforgreater flexibility in applications that requiredata and parameter storage.

Table 1   Memory Organization

| Block (64KB)	Block (32KB)	Sector (4KB)	AddressRange	
255	511	4095	FFF000h	FFFFFFh
	|	…	…	…
	510	4080	FF0000h	FF0FFFh
......	......	......	......	......
		......	......	......
		......	......	......
248	497	3983	F8F000h	F8FFFFh
	|	…	…	…
	496	3968	F80000h	F80FFFh
......	......	......	......	......
		......	......	......
		......	......	......
15	31	255	0FF000h	0FFFFFh
	|	…	…	…
	30	240	0F0000h	0F0FFFh
......	......	......	......	......
		......	......	......
		......	......	......
8	17	143	08F000h	08FFFFh
	|	…	…	…
	16	128	080000h	080FFFh
7	15	127	07F000h	07FFFFh
	|	…	…	…
	14	112	070000h	070FFFh
......	......	......	......	......
		......	......	......
		......	......	......
2	5	47	02F000h	02FFFFh
	|	…	…	…
	4	32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
	|	…	…	…
	2	16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
	|	…	…	…
	|	2	002000h	002FFFh
	0	1	001000h	001FFFh
		0	000000h	000FFFh

7. Device Operations
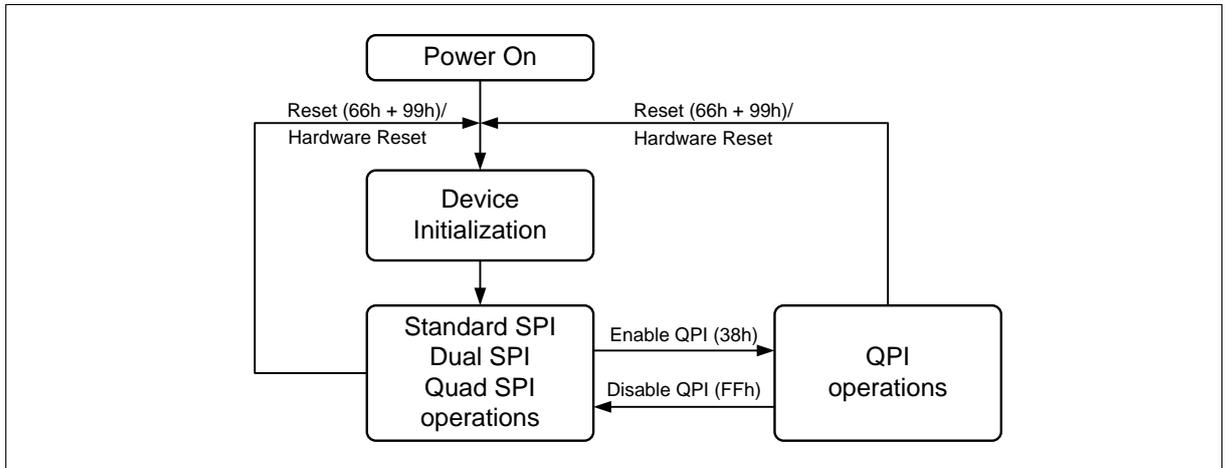
Figure 5   FM25LQ128I3 Serial Flash Memory Operation Diagram

7.1.   Standard SPI

The FM25LQ128I3 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device. The DO output pin is used to read data or status from the device.

Commands, write instructions, addresses or data are latched on the rising edge of CLK, read data or status are available on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.
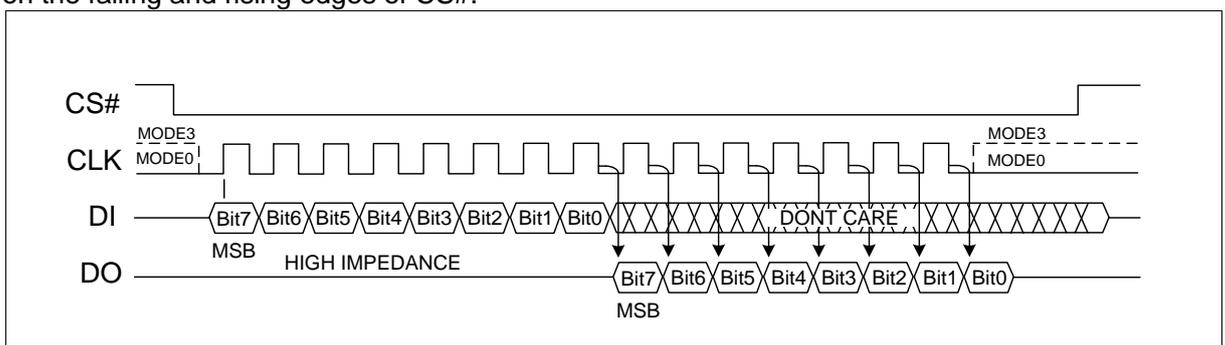
Figure 6   The difference between Mode 0 and Mode 3

7.2.   Dual SPI

The FM25LQ128I3 supports Dual SPI operation when using instructions such as "Fast Read Dual Output (3Bh)", "Fast Read Dual I/O (BBh)". These instructions allow data to be transferred to or from the device at twice the rate of the standard SPI. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ_0 and DQ_1.

7.3. Quad SPI

The FM25LQ128I3 supports Quad SPI operation when using instructions such as "Fast Read Quad Output (6Bh)", "Fast Read Quad I/O (EBh)". These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional DQ_0 and DQ_1 and the WP # and HOLD# pins become DQ_2 and DQ_3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

7.4. QPI

The FM25LQ128I3 supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the "Enable QPI (38h)" instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four DQ pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. "Enable QPI (38h)" and "Disable QPI (FFh)" instructions are used to switch between these two modes. Upon power-up or after a software reset using "Reset (66-99h)" instruction or hardware reset, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional DQ_0 and DQ_1, and the WP# and HOLD# pins become DQ_2 and DQ_3 respectively. See Figure 5 for the device operation modes.

7.5. SPI/QPI DTR Read Instruction

The FMLQ128I3supports multiple DTR (Double Transfer Rate) Read instructions that operate in Quad SPI and QPI modes to effectively improve the read operation throughput without increasing the serial clock frequency. The byte-long instruction code is still latched into the device onthe rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code isaccepted by the device, the address input and data output will be latched on both rising and falling edgesof the serial clock.

7.6. Hold

For Standard SPI and Dual SPI operations, the HOLD# signal allows the FM25LQ128I3 operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The HOLD# function is only available for standard SPI and Dual SPI operation, not during Quad SPI or QPI.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low theHOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.
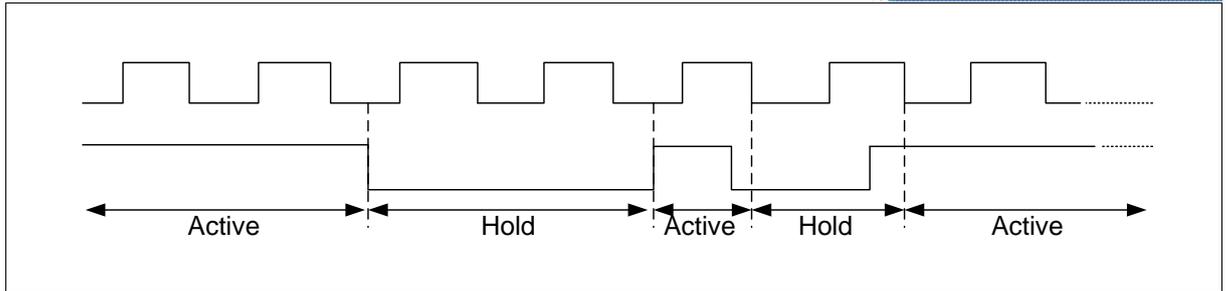
Figure 7   HoldCondition Waveform

7.7.   Software Reset& Hardware Reset

The FM25LQ128I3 can be reset to the initial power-on sate by a Software Reset sequence, either in SPI or QPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). No command will be accepted during the reset period.

FM25LQ128I3 can also be configured to utilize a hardware RESET# pin. The HOLD/RST bit in the Status Register-2 is the configuration bit for HOLD# pin function or RESET# pin function. When HOLD/RST=0 (factory default), the pin acts as a HOLD# pin as described above; when HOLD/RST=1, the pin acts as a RESET# pin. Drive the RESET# pin low for a minimum period of ~1us will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While RESET# is low, the device will not accept any command input.

If QE bit is set to 1, the HOLD# or RESET# function will be disabled, the pin will become one of the four data I/O pins.

Hardware RESET# pin has the highest priority among all the input signals. Drive RESET# low for a minimum period of ~1us will interrupt any on-going external/internal operations, regardless the status of other SPI signals (CS#, CLK, DI, DO, WP# and/or HOLD#).

Note:
1. While a faster RESET# pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum time is recommended to ensure reliable operation.
2. **Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when software/hardware reset is accepted by the device.** It is recommended to check the WIP bit and the SUS bit in Status Register before issuing the software reset command or hardware reset.

8.   Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the FM25LQ128I3 provides several means to protect the data from inadvertent writes.

Write Protect Features

- Device resets when VCC is below threshold during WRITE operation
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Status Register
- Advanced Sector Protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write-protection for array and Security Sectors using Status Register.

At power-up and power-down, the device must not be selected; that is, CS# must follow the voltage applied on VCC until VCC reaches the correct values: V_{CC} (min) at power-up and Vss at power-down.

To avoid data corruption and inadvertent WRITE operations during power-up, a power-on reset circuit is included. The logic inside the device is held to RESET while VCC is less than the power-on reset threshold voltage of V_{CC} (low); all operations are disabled, and the device does not respond to any instruction. During a standard power-up phase, the device ignores all commands. After power-up, the device is in standby power mode.

In the event Power-on Reset (POR) did not complete correctly after power up, the assertion of the RESET# signal or receiving a software reset command (RESET) will restart the POR process.

At power-down, when VCC drops from the operating voltage to below the threshold voltage V_{CC} (low), all operations are disabled and the device does not respond to any command.

Note: If power-down occurs while a WRITE, PROGRAM, or ERASE cycle is in progress, data corruption may result.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC, TB, BP[3:0]) bits. These settings allow a portion as small as a 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

The FM25LQ128I3 also provides another Write Protect method using the individual Block Locks. Each 64KB block (except the top and bottom blocks, total of 254 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with an Individual Block Lock bit. When the lock bit is 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, Erase or Program commands issued to the corresponding sector or block will be ignored. When the device is powered on, all individual Block Lock bits will be 1, so the entire memory array is protected from Erase/Program. An "Individual Block Unlock (39h)" instruction must be issued to unlock any specific sector or block.

The WPS bit in Status Register-2 is used to decide which Write Protect scheme should be used. When WPS=0(factory default), the device will only utilize CMP,SEC,TB, BP[2:0] to protect specific areas of the array; when WPS=1, the device will utilize the Individual Block Locksfor write protection, each protect scheme for the corresponding is available.

9. Status Register

Three Status Registers are provided for FM25LQ128I3. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the Flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Sector lock status, Erase/Program Suspend status and output driver strength. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Sector OTP lock, Hold/RESET functions and output driver strength. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and during Standard/Dual SPI operations, the WP# pin.

Factory default for all Status Register bits are 0.

9.1. Status Register-1(SR1)

Related Commands: Read Status Register (RDSR1 05h), Write Status Register (WRSR 01h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Enable for Volatile Status Register(50h).

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	SEC	TB	BP2	BP1	BP0	WEL	WIP

STATUS REGISTER PROTECT 0
(Volatile/Non-Volatile writable)

SECTOR PROTECT BIT
(Volatile/Non-Volatile writable
should be set to 0)

TOP/BOTTOM PROTECT
(Volatile/Non-Volatile writable)

BLOCK PROTECT BITS
(Volatile/Non-Volatile writable)

WRITE ENABLE LATCH

ERASE/WRITE IN PROGRESS
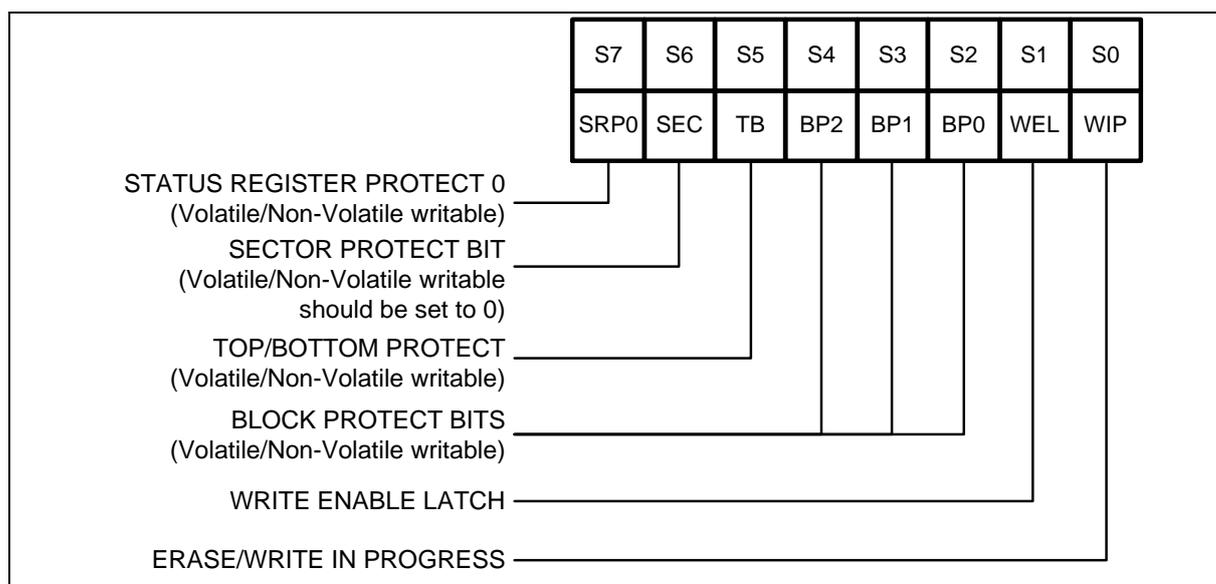
Figure 8 Status Register-1

9.1.1. Write In Progress(WIP)

WIP is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Sector instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in "11.6AC Electrical Characteristics"). When the program, erase or write status register(or securitysector) instruction has completed, the WIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

9.1.2. Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disablestateoccursuponpower-uporafteranyofthe following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Sector and Program Security Sector.

9.1.3. Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status registerthat provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in "11.6AC Electrical Characteristics"). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection). The factory default setting for the Block Protection Bits is 0, none of the array protected.

9.1.4. Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

9.1.5. Sector/Block Protect (SEC)

The non-volatile Sector/Block Protect bit (SEC) should be set to 0. The factory default setting is SEC=0.

9.2. Status Register-2 (SR2)

Related Commands: Read Status Register-2 (RDSR2 35h), Write Status Register-2 (WRSR2 31h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Enable for Volatile Status Register (50h).
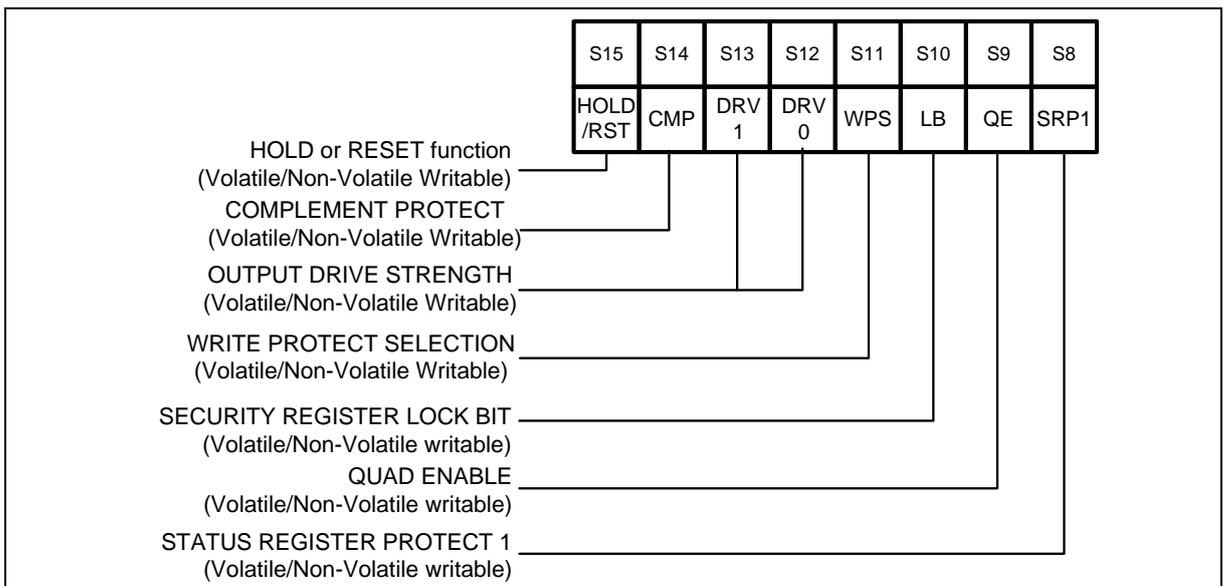

Figure 9   Status Register-2

9.2.1. Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register   (S8andS7).TheSRPbitscontrolthemethodofwriteprotection:softwareprotection,hardware protection, power supply lock-down or one time programmable (OTP) protection.

Table 2   Status Register Protect bits

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protection	WP# pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. (Factory Default)
0	1	0	Hardware Protected	When WP# pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When WP# pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and can not be written to again until the next power-down, power-up cycle.[1]
1	1	X	One Time Program	Status Register is permanently protected and can not be written to.

Note:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

9.2.2. HOLD# or RESET# pin function(HOLD/RST)

The HOLD/RST bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as HOLD#; when HOLD/RST=1, the pin acts as RESET#. However, HOLD# or RESET# functions are only available when QE=0. If QE is set to 1, the HOLD# and RESET# functions are disabled, the pin acts as a dedicated data I/O pin.

9.2.3. Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP[2:0] bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to Status Register Memory Protection table for details. The default setting is CMP=0.

9.2.4. Write Protect Selection (WPS)

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, TB, SEC, BP[2:0] to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

9.2.5. Output driver strength (DRV1, DRV0)

The DRV1 & DRV0 bits are used to determine the output driver strength.

Table 3 Driver strength configuration

DRV1, DRV0	Driver Strength
0,0	100%
1,0	75%
0,1	50%
1,1	25%

9.2.6. Security Sector Lock Bit (LB)

The Security Register Lock Bit (LB) is non-volatile One Time Program (OTP) bits in Status Register (S10) that provide the write protect control and status to the Security Registers. The default state of LB is 0, Security Registers are unlocked. LBcan be set to 1 individually using the Write Status Register instruction. LBis One Time Programmable (OTP), once it's set to 1, the corresponding 1024-Byte Security Register will become read-only permanently.

9.2.7. Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state, the WP# pin and HOLD# are enabled. When the QE bit is set to a 1, the Quad DQ2 and DQ3 pins are enabled, and WP# and HOLD# functions are disabled.

QE bit is required to be set to a 1 before issuing an "Enable QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI; otherwise the command will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A "Write Status Register" command in QPI mode cannot change QE bit from a 1 to a 0.

WARNING: If the WP# or HOLD# pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

9.3. Status Register-3 (SR3)

Related Commands: Read Status Register-3 (RDSR3 15h), Write Enable (06h).Write Enable (06h) can be used to clear ERR bit of SR3 if ERR is set to 1 by the last operation.
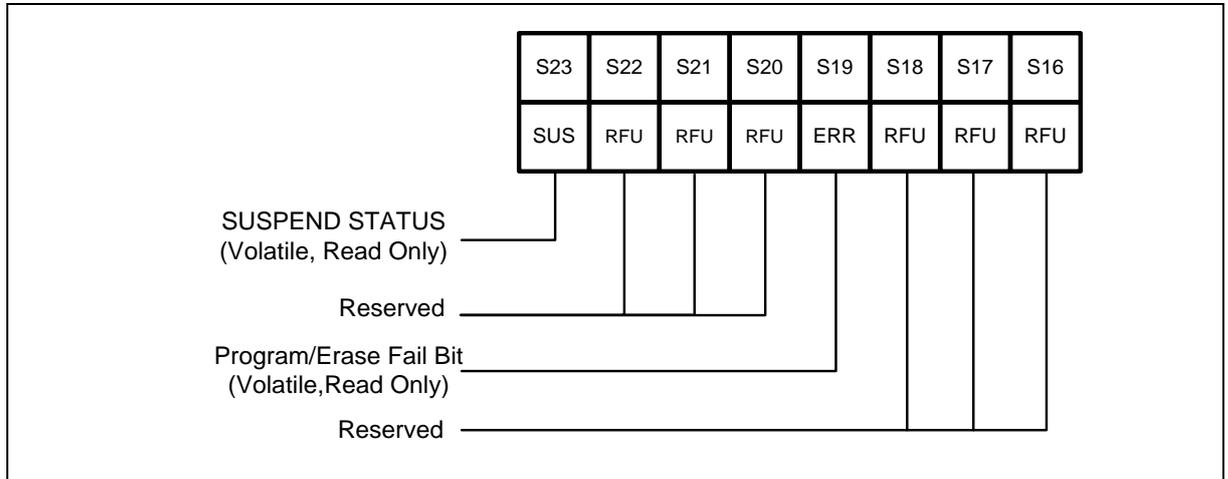

Figure 10 Status Register-3

9.3.1. Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S23) that is set to 1 after executing an Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

9.3.2. Write Fail Bit (ERR)

The Write Fail bit is a status flag, which shows the status of last write operation. It will be set to 1, if the program or erase or write status register operation fails. It is cleard to 0 by WREN (06h) or Reset operation.

9.4. Status Register Memory Protection(WPS=0, CMP=0)

Table 4   Status Register Memory Protection (WPS=0, CMP=0)

STATUS REGISTER					FM25LQ128I3 (128M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 thru 255	FC0000h – FFFFFFh	256KB	Upper 1/64
0	0	0	1	0	248 thru 255	F80000h – FFFFFFh	512KB	Upper 1/32
0	0	0	1	1	240 thru 255	F00000h – FFFFFFh	1MB	Upper 1/16
0	0	1	0	0	224 thru 255	E00000h – FFFFFFh	2MB	Upper 1/8
0	0	1	0	1	192 thru 255	C00000h – FFFFFFh	4MB	Upper 1/4
0	0	1	1	0	128 thru 255	800000h – FFFFFFh	8MB	Upper 1/2
0	1	0	0	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/64
0	1	0	1	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/32
0	1	0	1	1	0 thru 15	000000h – 0FFFFFh	1M	Lower 1/16
0	1	1	0	0	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/8
0	1	1	0	1	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/4
0	1	1	1	0	0 thru 127	000000h – 7FFFFFh	8MB	Lower 1/2
X	X	1	1	1	0 thru 255	000000h – FFFFFFh	16MB	ALL
1	0	0	0	1	255	FFF000h – FFFFFFh	4KB	Upper 1/4096
1	0	0	1	0	255	FFE000h – FFFFFFh	8KB	Upper 1/2048
1	0	0	1	1	255	FFC000h – FFFFFFh	16KB	Upper 1/1024
1	0	1	0	X	255	FF8000h – FFFFFFh	32KB	Upper 1/512
1	0	1	1	0	255	FF8000h – FFFFFFh	32KB	Upper 1/512
1	1	0	0	1	0	000000h – 000FFFh	4KB	Lower 1/4096
1	1	0	1	0	0	000000h – 001FFFh	8KB	Lower 1/2048
1	1	0	1	1	0	000000h – 003FFFh	16KB	Lower 1/1024
1	1	1	0	X	0	000000h – 007FFFh	32KB	Lower 1/512
1	1	1	1	0	0	000000h – 007FFFh	32KB	Lower 1/512

9.5. Status Register Memory Protection(WPS=0, CMP=1)

Table 5   Status Register Memory Protection (WPS=0, CMP=1)

STATUS REGISTER					FM25LQ128I3 (128M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	X	0	0	0	0 to 255	000000h – FFFFFFh	ALL	ALL
0	0	0	0	1	0 to 255	000000h – FBFFFFh	16128KB	Lower 63/64
0	0	0	1	0	0 to 255	000000h – F7FFFFh	15872KB	Lower 31/32
0	0	0	1	1	0 to 255	000000h – EFFFFFh	15MB	Lower 15/16
0	0	1	0	0	0 to 255	000000h – DFFFFFh	14MB	Lower 7/8
0	0	1	0	1	0 to 255	000000h – BFFFFFh	12MB	Lower 3/4
0	0	1	1	0	0 to 255	000000h – 7FFFFFh	8MB	Lower 1/2
0	1	0	0	1	4 to 255	040000h – FFFFFFh	16128KB	Upper 63/64
0	1	0	1	0	8 to 255	080000h – FFFFFFh	15872KB	Upper 31/32
0	1	0	1	1	16 to 255	100000h – FFFFFFh	15MB	Upper 15/16
0	1	1	0	0	32 to 255	200000h – FFFFFFh	14MB	Upper 7/8
0	1	1	0	1	64 to 255	400000h – FFFFFFh	12MB	Upper 3/4
0	1	1	1	0	128 to 255	800000h – FFFFFFh	8MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 255	000000h – FFEFFFh	16380KB	L-4095/4096
1	0	0	1	0	0 to 255	000000h – FFDFFFh	16376KB	L-2047/2048
1	0	0	1	1	0 to 255	000000h – FFBFFFh	16368KB	L-1023/1024
1	0	1	0	X	0 to 255	000000h – FF7FFFh	16352KB	L-511/512
1	0	1	1	0	0 to 255	000000h – FF7FFFh	16352KB	L-511/512
1	1	0	0	1	0 to 255	001000h – FFFFFFh	16380KB	U-4095/4096
1	1	0	1	0	0 to 255	002000h – FFFFFFh	16376KB	U-2047/2048
1	1	0	1	1	0 to 255	004000h – FFFFFFh	16368KB	U-1023/1024
1	1	1	0	X	0 to 255	008000h – FFFFFFh	16352KB	U-511/512
1	1	1	1	0	0 to 255	008000h – FFFFFFh	16352KB	U-511/512

9.6. Status Register Memory Protection (WPS=1)

```
Block 255
(64KB)          Sector 15(4KB)  ←────────┐
                Sector 14(4KB)  ←────────┤
                     ⋮
                Sector 1(4KB)   ←────────┤
                Sector 0(4KB)   ←────────┤
                                          │
                Block 254(64KB) ←────────┤
                     ⋮                   │
                                          │
                Block 1(64KB)   ←────────┤
Block 0
(64KB)          Sector 15(4KB)  ←────────┤
                Sector 14(4KB)  ←────────┤
                     ⋮                   │
                Sector 1(4KB)   ←────────┤
                Sector 0(4KB)   ←────────┘
```

Individual Block Locks:
32 Sectors(Top/Bottom)
254 Blocks

Individual Block Lock:
36h + Address

Individual Block Unlock:
39h + Address

Read Block Lock:
3Dh + Address

Global Block Lock:
7Eh

Global Block Unlock:
98h
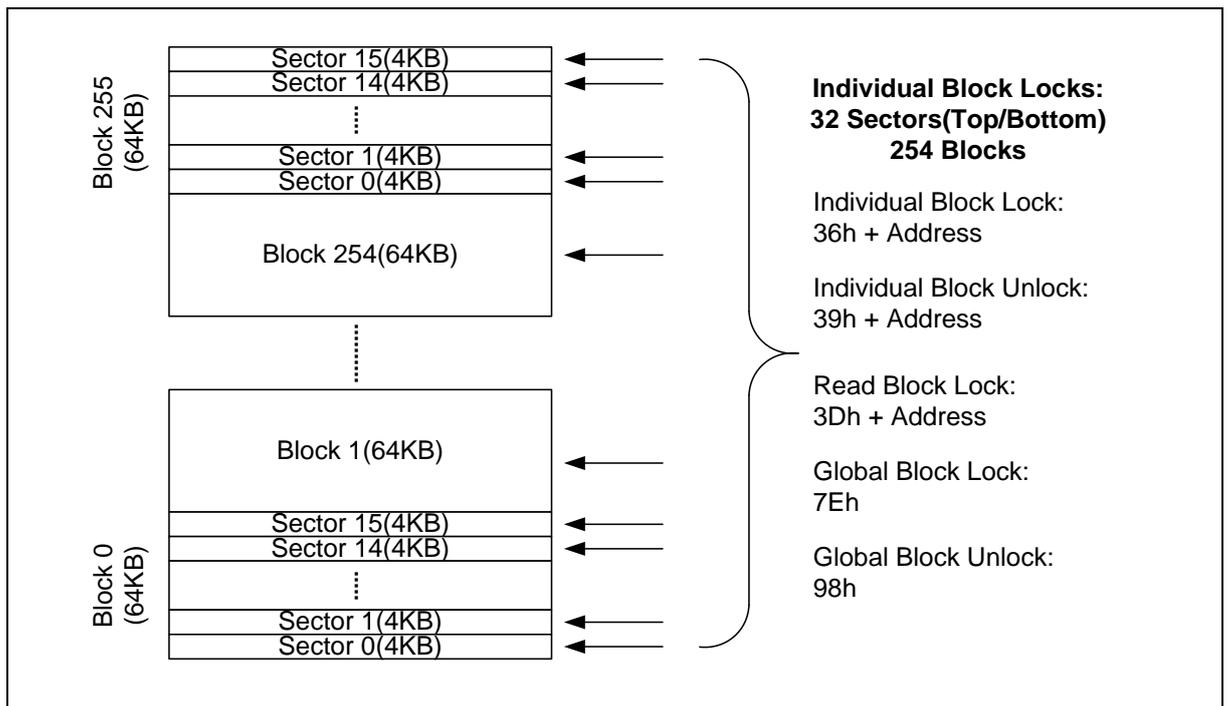
Figure 11 Individual Sector/Block Locks

10. Instructions

The Standard/Dual/Quad SPI instruction set of the FM25LQ128I3 consists of 44 basic instructions that are fully controlled through the SPI bus (see Table 7 ~ Table 10Instruction Set). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI instruction set of the FM25LQ128I3 consists of 30 basic instructions that are fully controlled through the SPI bus (seeTable 10 Instruction Set). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked through DQ[3:0] pins provides the instruction code. Data on all four DQ pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI instructions, addresses, data and dummy bytes are using all four DQ pins to transfer every byte of data with every two serial clocks (CLK).

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of CS#. Clock relative timing diagrams for each instruction are included in Figure 12 through Figure 83. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

10.1. Device ID and Instruction Set Tables

10.1.1. Manufacture and Device Identification

Table 6   Manufacturer and Device Identification

OP Code	MF7-MF0	ID15-ID0	ID7-ID0
ABh			17h
90h,92h,94h	A1h		17h
9Fh	A1h	6018h	

10.1.2. Standard SPI Instructions Set

Table 7   Standard SPI Instructions Set [1]

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Write Enable	**06h**					
Volatile SR Write Enable	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7-S0)[2]				
Write Status Register-1[3]	**01h**	(S7-S0)[3]				
Read Status Register-2	**35h**	(S15-S8)[2]				
Write Status Register-2	**31h**	(S15-S8)				
Read Status Register-3	**15h**	(S23-S16)[2]				
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0[4]
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**C7h/60h**					
Erase / Program Suspend	**75h**					
Erase / Program Resume	**7Ah**					
Power-down	**B9h**					
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Release Powerdown / ID[5]	**ABh**	dummy	dummy	Dummy	(ID7-ID0)[2]	
Manufacturer/Device ID[5][6]	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID[6]	**9Fh**	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
Read SFDP Register	**5Ah**	00h	00h	A7-A0	dummy	(D7-D0)
Read Unique ID[6]	**4Bh**	dummy	dummy	dummy	dummy	(UID63-UID0)
Erase Security Sectors[7]	**44h**	A23-A16	A15-A8	A7-A0		
Program Security Sectors[7]	**42h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0
Read Security Sectors[7]	**48h**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Enable QPI	**38h**					
Enable Reset	**66h**					
Reset	**99h**					
Individual Block Lock	**36h**	A23-A16	A15-A8	A7-A0		
Individual Block Unlock	**39h**	A23-A16	A15-A8	A7-A0		
Read Block Lock	**3Dh**	A23-A16	A15-A8	A7-A0		
Global Block Lock	**7Eh**	A23-A16	A15-A8	A7-A0		
Global Block Unlock	**98h**	A23-A16	A15-A8	A7-A0		

10.1.3. Dual SPI Instructions Set

Table 8   Dual SPI Instructions Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)[9]
Fast Read Dual I/O	**BBh**	A23-A8[8]	A7-A0, M7-M0 [8]	Dummy	(D7-D0, …)[9]	
Manufacturer/Device ID by Dual I/O[5][6]	**92h**	A23-A8[8]	A7-A0, M7-M0[8]	(MF7-MF0, ID7-ID0)		

10.1.4. Quad SPI Instructions Set

Table 9   Quad SPI Instructions Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Quad Page Program	**32h**	A23-A16	A15-A8	A7-A0	D7-D0, …[11]	D7-D0, …[11]
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)[11]
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0[10]	Dummy[13]	(D7-D0, …)[11]		
Set Burst with Wrap	**77h**	xxxxx, W6-W4[10]				
Manufacture/Device ID by Quad I/O[5][6]	**94h**	A23-A0, M7-M0[10]	xxxx, (MF7-MF0, ID7-ID0)	(MF7-MF0, ID7-ID0, …)		

10.1.5. QPI Instructions Set

Table 10   QPI Instructions Set[12]

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0,1)*	*(2,3)*	*(4,5)*	*(6,7)*	*(8,9)*	*(10,11)*
Write Enable	**06h**					
Volatile SR Write Enable	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7-S0)[2]				
Write Status Register-1[3]	**01h**	(S7-S0)[3]				
Read Status Register-2	**35h**	(S15-S8)[2]				
Write Status Register-2	**31h**	(S15-S8)				
Read Status Register-3	**15h**	(S23-S16)[2]				
Chip Erase	**C7h/60h**					
Erase / Program Suspend	**75h**					
Erase / Program Resume	**7Ah**					
Power-down	**B9h**					
Set Read Parameters	**C0h**	P7-P0				
Enable Reset	**66h**					
Reset	**99h**					
Disable QPI	**FFh**					
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy[13]	(D7-D0)
Burst Read with Wrap	**0Ch**	A23-A16	A15-A8	A7-A0	dummy[13]	(D7-D0)
Fast Read Quad I/O[14]	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0[13]	(D7-D0)
Release Powerdown / ID[5]	**ABh**	dummy	dummy	dummy	(ID7-ID0)[2]	
Manufacturer/Device ID[5][6]	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID[5][6]	**9Fh**	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0[11]	D7-D0[4]
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Individual Block Lock	**36h**	A23-A16	A15-A8	A7-A0		
Individual Block Unlock	**39h**	A23-A16	A15-A8	A7-A0		
Read Block Lock	**3Dh**	A23-A16	A15-A8	A7-A0	(D7-D0)[2]	
Global Block Lock	**7Eh**	A23-A16	A15-A8	A7-A0		
Global Block Unlock	**98h**	A23-A16	A15-A8	A7-A0		

10.1.6. DTR Instructions Set

Table 11   DTR Instructions Set(Quad SPI, QPI)

DTR Fast Read Quad I/O	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	(0-7)	(8)	(9)	(10)	(11)	(12-20)
Quad SPI	EDh	A23-A16	A15-A8	A7-A0	M7-M0	dummy
CLOCK NUMBER	(0,1)	(2)	(3)	(4)	(5)	(6-n)[13]
QPI	EDh	A23-A16	A15-A8	A7-A0	M7-M0	dummy

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 DQ pins.
2. The Status Register contents and Device ID will repeat continuously until CS# terminates the instruction.
3. Write Status Register-1(01h) can also be used to program Status Register-1&2, see section 10.2.5
4. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Sectors, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
5. See Table 6Manufacturer and Device Identification table for device ID information.
6. Please contact Shanghai Fudan Microelectronics Group Co., Ltd for details.
7. Security Sector Address:
   Security Sector 0: A23-A16 = 00h; A15-A8 = 00h; A7-A0 = byte address
   Security Sector 1: A23-A16 = 00h; A15-A8 = 01h; A7-A0 = byte address
   Security Sector 2: A23-A16 = 00h; A15-A8 = 10h; A7-A0 = byte address
   Security Sector 3: A23-A16 = 00h; A15-A8 = 11h; A7-A0 = byte address
8. Dual SPI address input format:
   DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
9. Dual SPI data output format:
   DQ_0 = (D6, D4, D2, D0)
   DQ_1 = (D7, D5, D3, D1)
10. Quad SPI address input format: Set Burst with Wrap input format:
    DQ_0 = A20, A16, A12, A8, A4, A0, M4, M0 DQ_0 = x, x, x, x, x, x, W4, x
    DQ_1 = A21, A17, A13, A9, A5, A1, M5, M1 DQ_1 = x, x, x, x, x, x, W5, x
    DQ_2 = A22, A18, A14, A10, A6, A2, M6, M2 DQ_2 = x, x, x, x, x, x, W6, x
    DQ_3 = A23, A19, A15, A11, A7, A3, M7, M3 DQ_3 = x, x, x, x, x, x, x,   x
11. Quad SPI data input/output format:
    DQ_0 = (D4, D0 …)
    DQ_1 = (D5, D1…)
    DQ_2 = (D6, D2…)
    DQ_3 = (D7, D3…)
12. QPI Command Address, Data input/output format:

CLK#	0	1	2	3	4	5	6	7	8	9	10	11
DQ_0	C4	C0	A20	A16	A12	A8	A4	A0	D4	D0	D4	D0
DQ_1	C5	C1	A21	A17	A13	A9	A5	A1	D5	D1	D5	D1
DQ_2	C6	C2	A22	A18	A14	A10	A6	A2	D6	D2	D6	D2
DQ_3	C7	C3	A23	A19	A15	A11	A7	A3	D7	D3	D7	D3

13. The number of dummy clocks is controlled by read parameter P5-P4.
14. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P1-P0

10.2. Instruction Description

10.2.1. Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 12) sets the Write Enable Latch (WEL) bit in the Status Register to a1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase/Program Security Sectors and Block/Sector Lock/Unlock instruction. The Write Enable **(**WREN**)** instruction is entered by driving CS# low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.
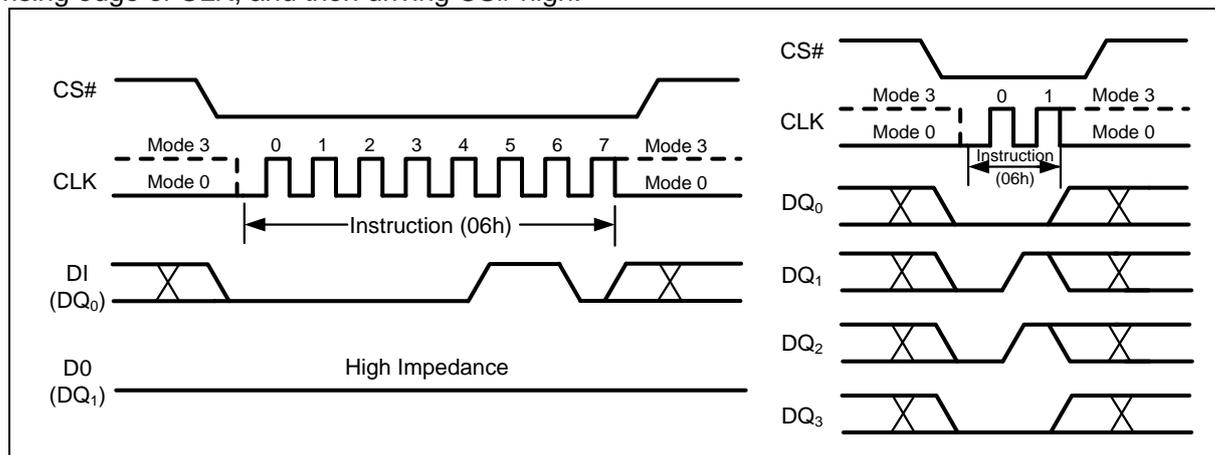
Figure 12 Write Enable Instruction for SPI Mode (left) or QPI Mode (right)

10.2.2. Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 9.1, 9.2, 9.3 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 13) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.
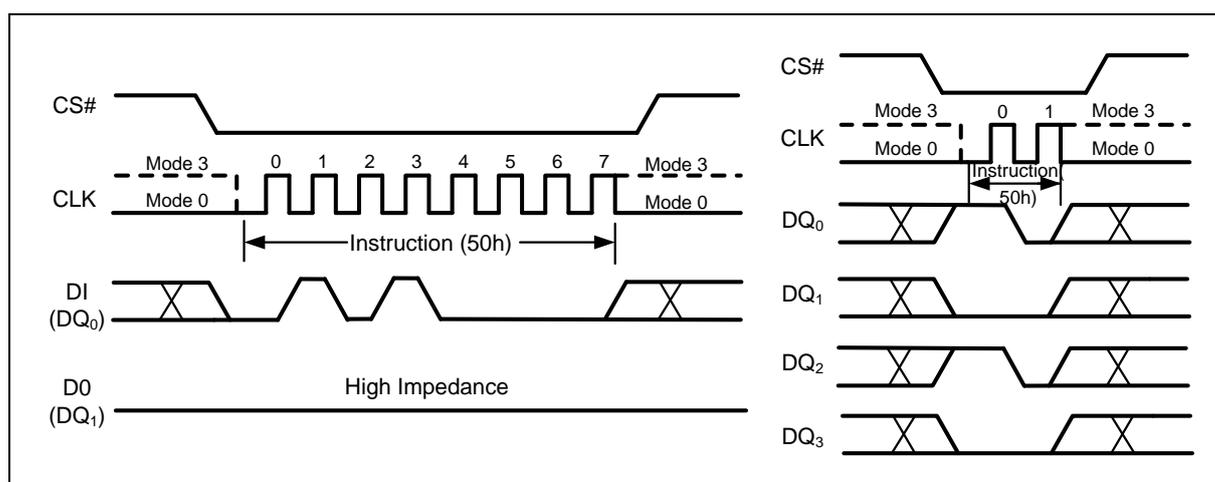
Figure 13 Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)

10.2.3. Write Disable(WRDI) (04h)

The Write Disable (WRDI) instruction (Figure 14) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable(WRDI) instruction is entered by driving CS# low, shifting the instruction code "04h" into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Sectors, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase ,Block/Sector Lock/Unlock and Reset instructions.
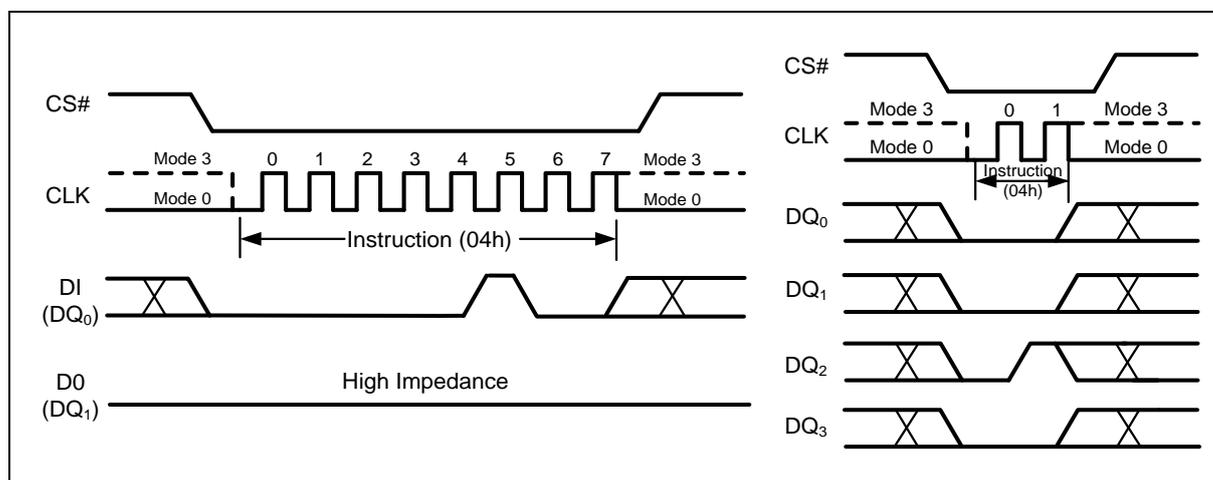
Figure 14 Write Disable Instruction for SPI Mode (left) or QPI Mode (right)

10.2.4. Read Status Register-1(RDSR1) (05h), Status Register-2 (RDSR2)(35h) &Status Register-3 (RDSR3) (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving CS# low and shifting the instruction code "05h"for Status Register-1, "35h" for Status Register-2 or "15h" for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 15. Refer to section 9.1, 9.2 and 9.3 for Status Register description.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 16. The instruction is completed by driving CS# high.
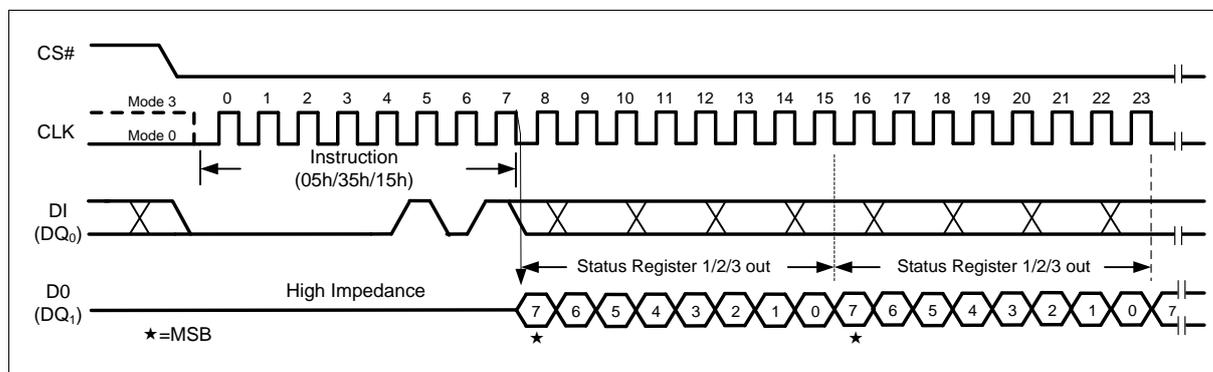
Figure 15 Read Status Register Instruction (SPI Mode)
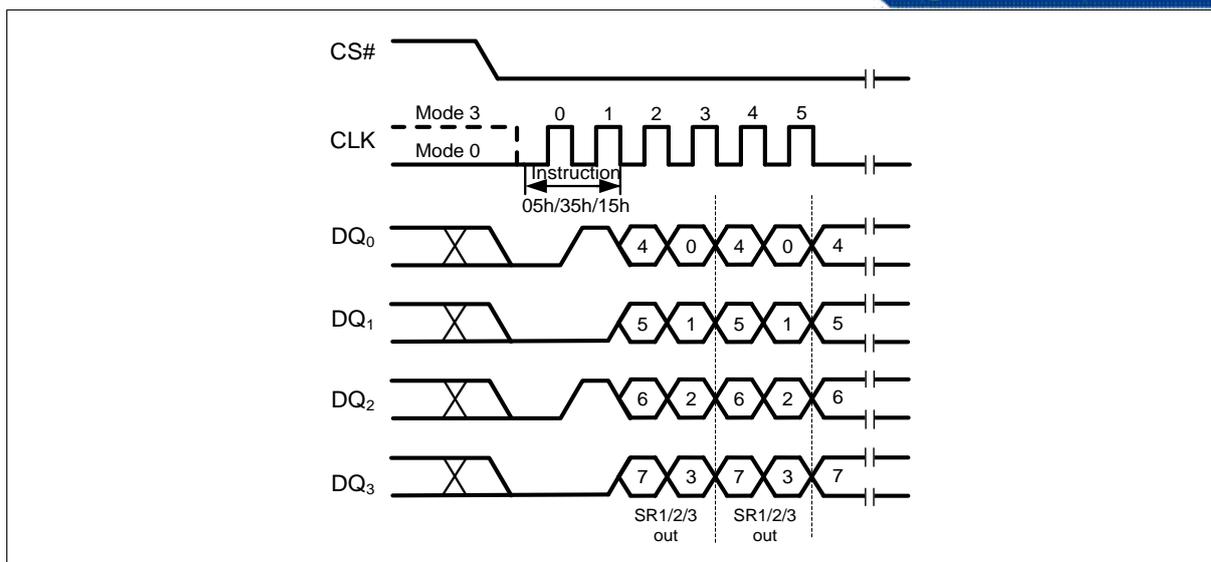
Figure 16 Read Status Register Instruction (QPI Mode)

10.2.5. Write Status Register-1 (WRSR1)(01h), Status Register-2(WRSR2) (31h)

The Write Status Register instruction allows the Status Register to be written. The writable Status Register bits include: SRP0, TB, SEC, BP2, BP1 and BP0 in Status Register-1; HOLD/RST, CMP, LB, QE, SRP1, DRV1, DRV0 and WPS in Status Register-2. All other Status Register bit locations are read-only and will not be affected by Write Status Register instruction. LB is a non-volatile OTP bit, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Registerinstruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code "01h/31h", and then writing the status register data byte as illustrated inFigure 17&Figure 18.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRP1 and LBcannot be changed from 1 to 0 because of the OTP protection for these bits. Upon power off or the execution of Software Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See "11.6AC Electrical Characteristics"). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h), after CS# is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2}(See "11.6AC Electrical Characteristics"). WIP bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to 0 when the device is in the QPI mode, because QE=1 is required

for the device to enter and operate in the QPI mode.

Refer to section 9.1, 9.2, 9.3 for Status Register description. Factory default for all status Register bits are 0.
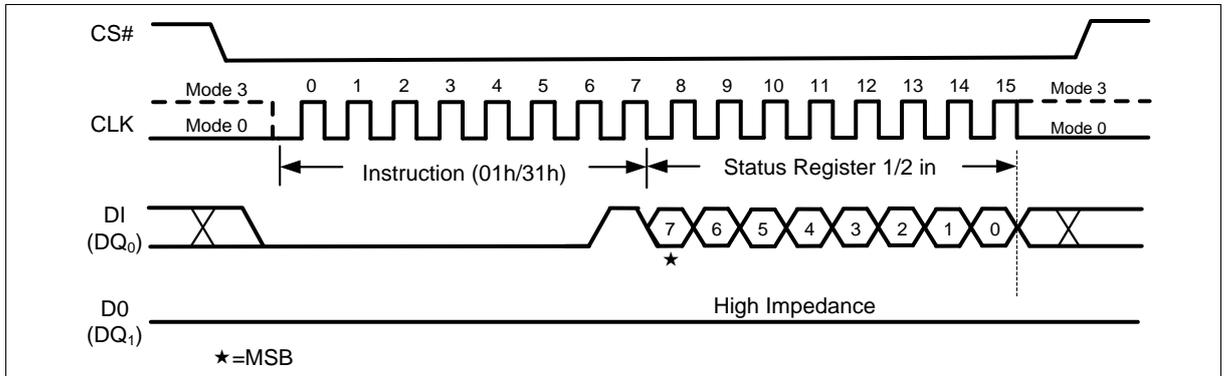
Figure 17 Write Status Register-1/2 Instruction (SPI Mode)
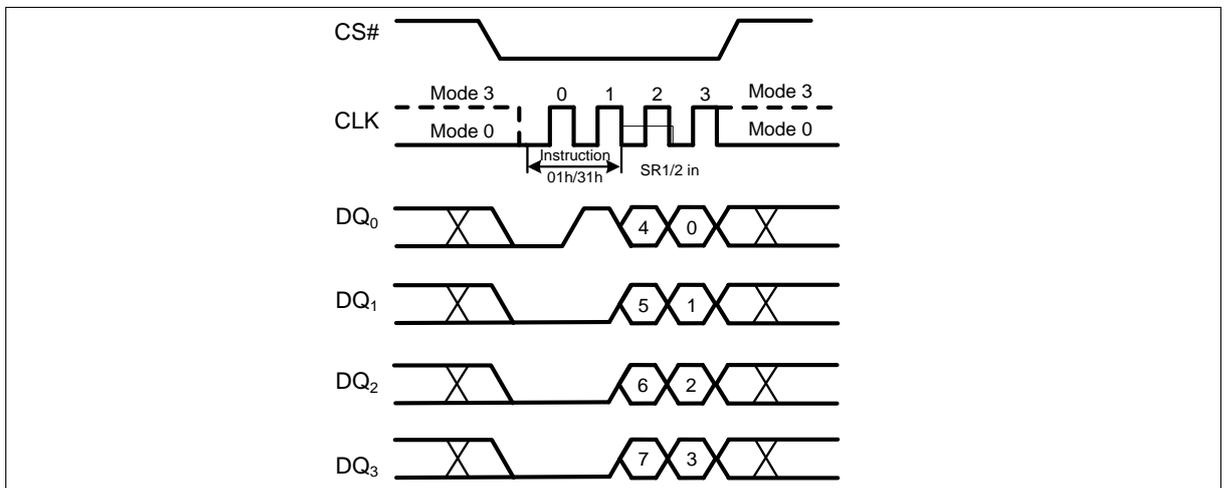
Figure 18 Write Status Register-1/2 Instruction (QPI Mode)

The FM25LQ128I3 is also backward compatible to FMSH's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Register-1(01h)" command. To complete the Write Status Register1&2, the CS# pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 19. If CS# is driven high after the eighth clock, the Write Status Register (WRSR) instruction will only program the Status Register-1 and the Status Register-2 will not be affected.
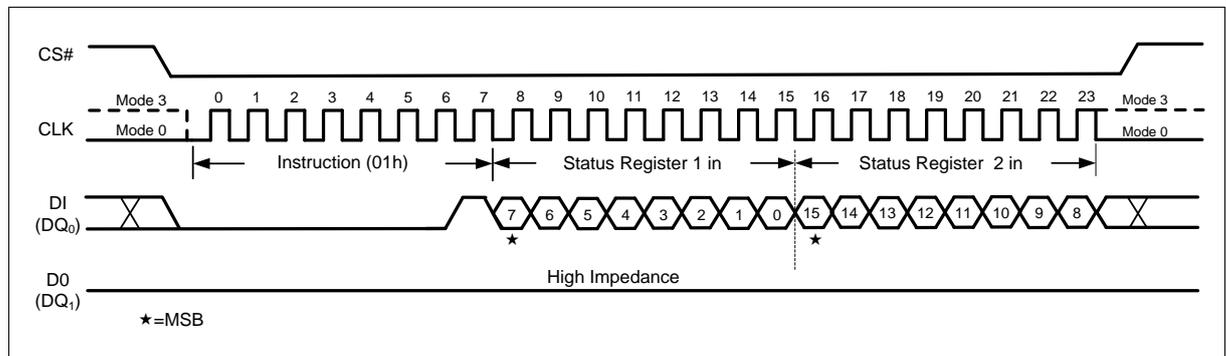
Figure 19 Write Status Register-1/2 Instruction (backward compatible,SPI Mode)
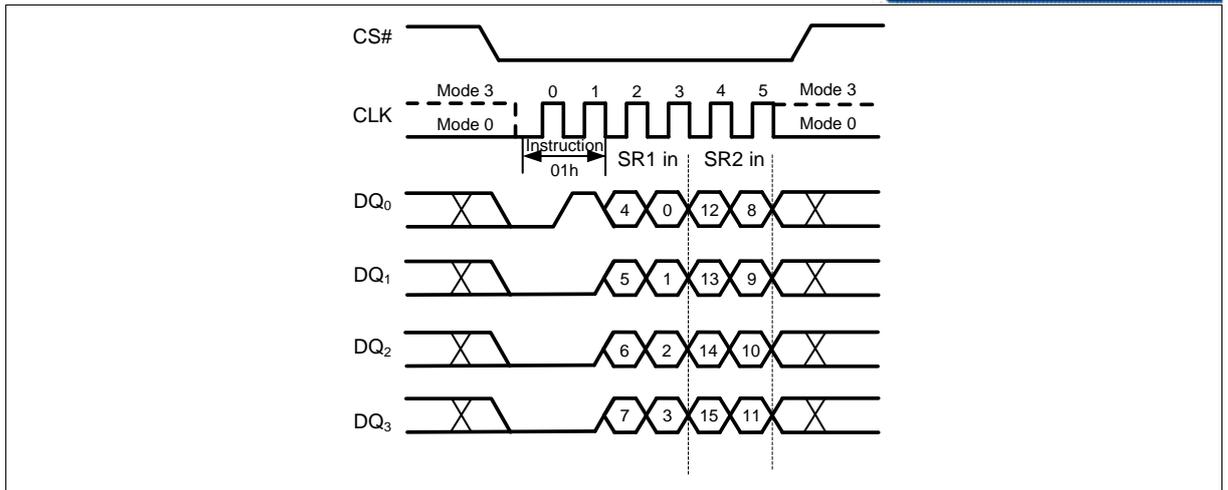
Figure 20 Write Status Register-1/2 Instruction (backward compatible,QPI Mode)

10.2.6. Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code "03h" followed by a24-bit address A23-A0 into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in Figure 21. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (WIP =1) the instruction is ignored and will not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see "11.6AC Electrical Characteristics").

The Read Data (03h) instruction is only supported in Standard SPI mode.
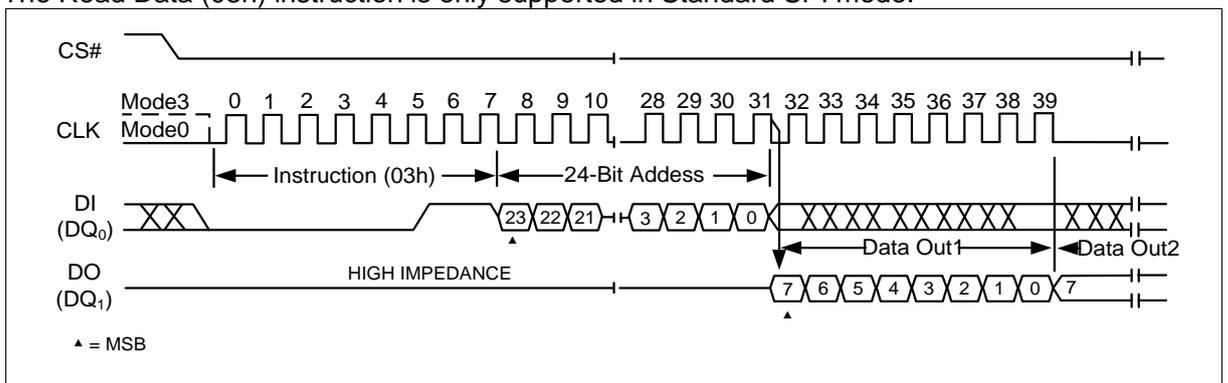
Figure 21 Read Data Instruction (SPI Mode only)

10.2.7. Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R(see "11.6AC Electrical Characteristics"). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 22. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DI pin is a "don't care".
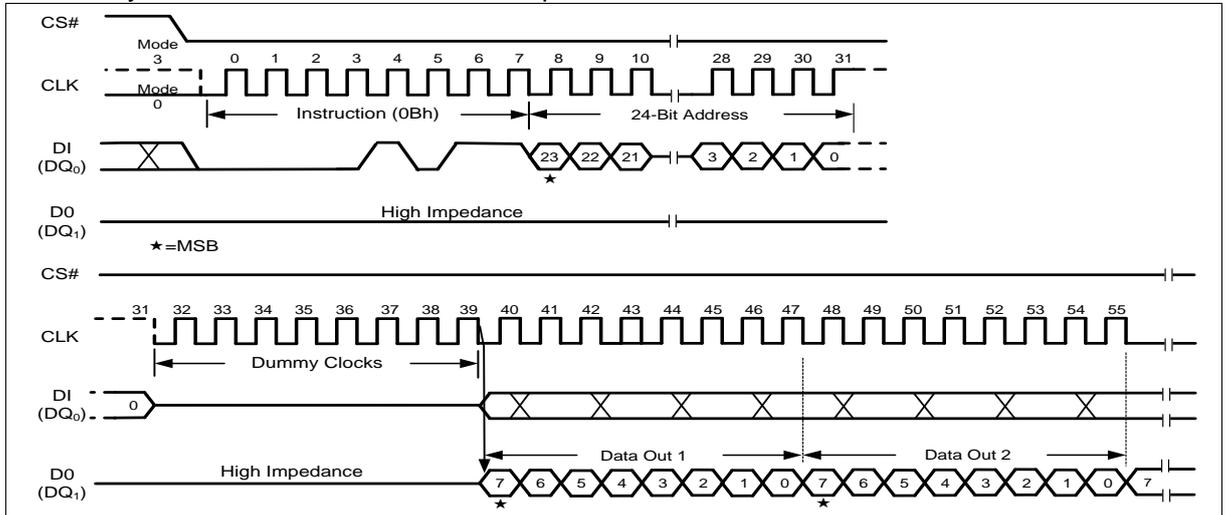
Figure 22 Fast Read Instruction (SPI Mode)

Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.
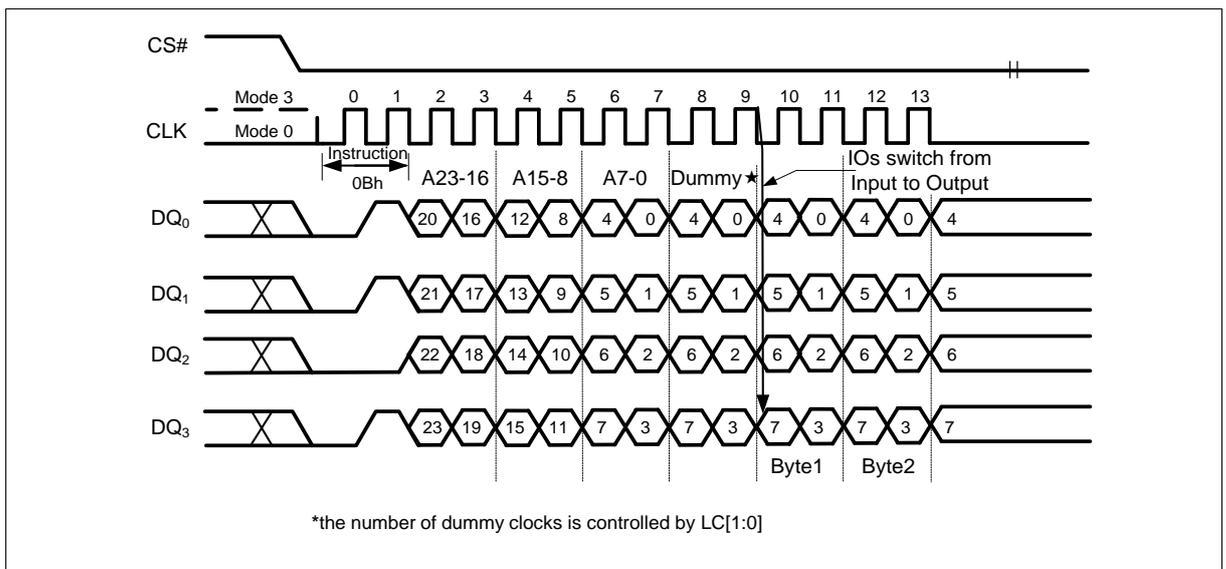
Figure 23 Fast Read Instruction (QPI Mode)

10.2.8. Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; DQ_0 and DQ_1. This allows data to be transferred from the FM25LQ128I3 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R(see "11.6AC Electrical Characteristics"). For Fast Read Dual Output instruction, there are eight dummy cycles required after the last address bit is shifted into DI before data begins shifting out of DQ_0 and DQ_1. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DQ_0 pin should be high-impedance prior to the falling edge of the first data out clock.
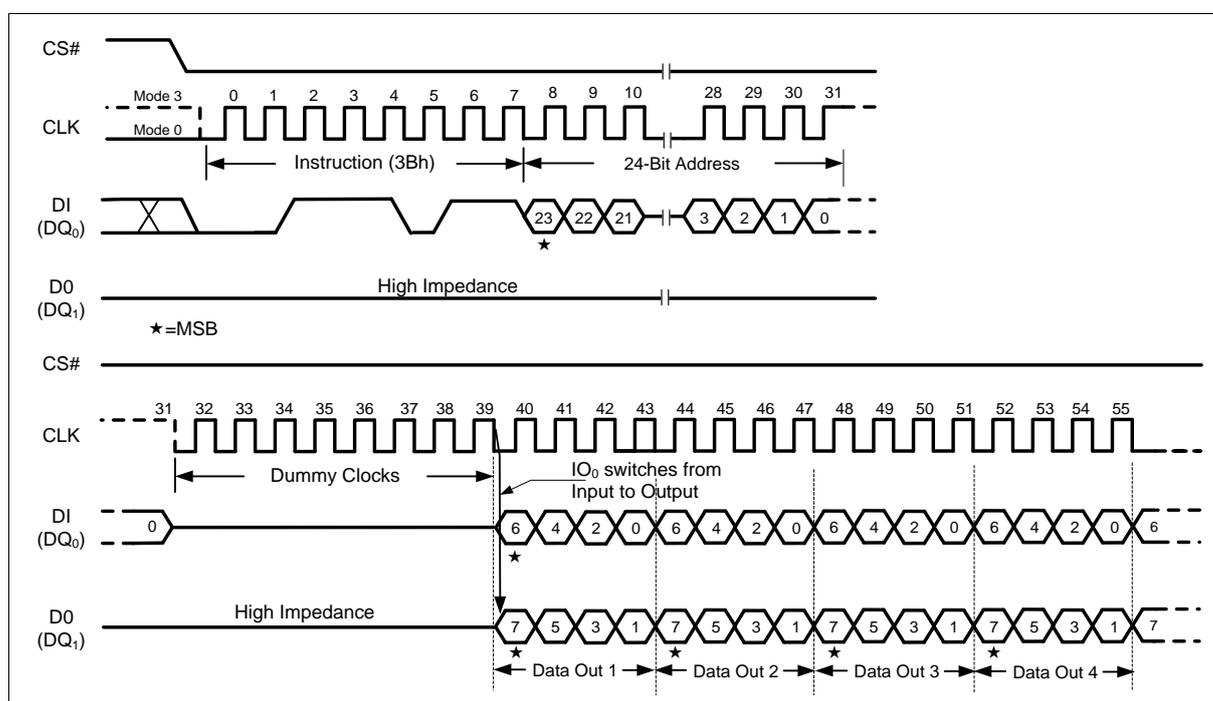
Figure 24   Fast Read Dual Output Instruction (SPI Mode only)

10.2.9. Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, DQ_0, DQ_1, DQ_2, and DQ_3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Instruction (Status Register bit QE mustequal1).TheFastReadQuadOutputInstructionallowsdatatobetransferredfrom the FM25LQ128I3 at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of F_R (see "11.6AC Electrical Characteristics"). For Fast Read Quad Output instruction, there are eight dummy cycles required after the last address bit is shifted into DI before data begins shifting out of DQ_0, DQ_1, DQ_2 and DQ_3. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.
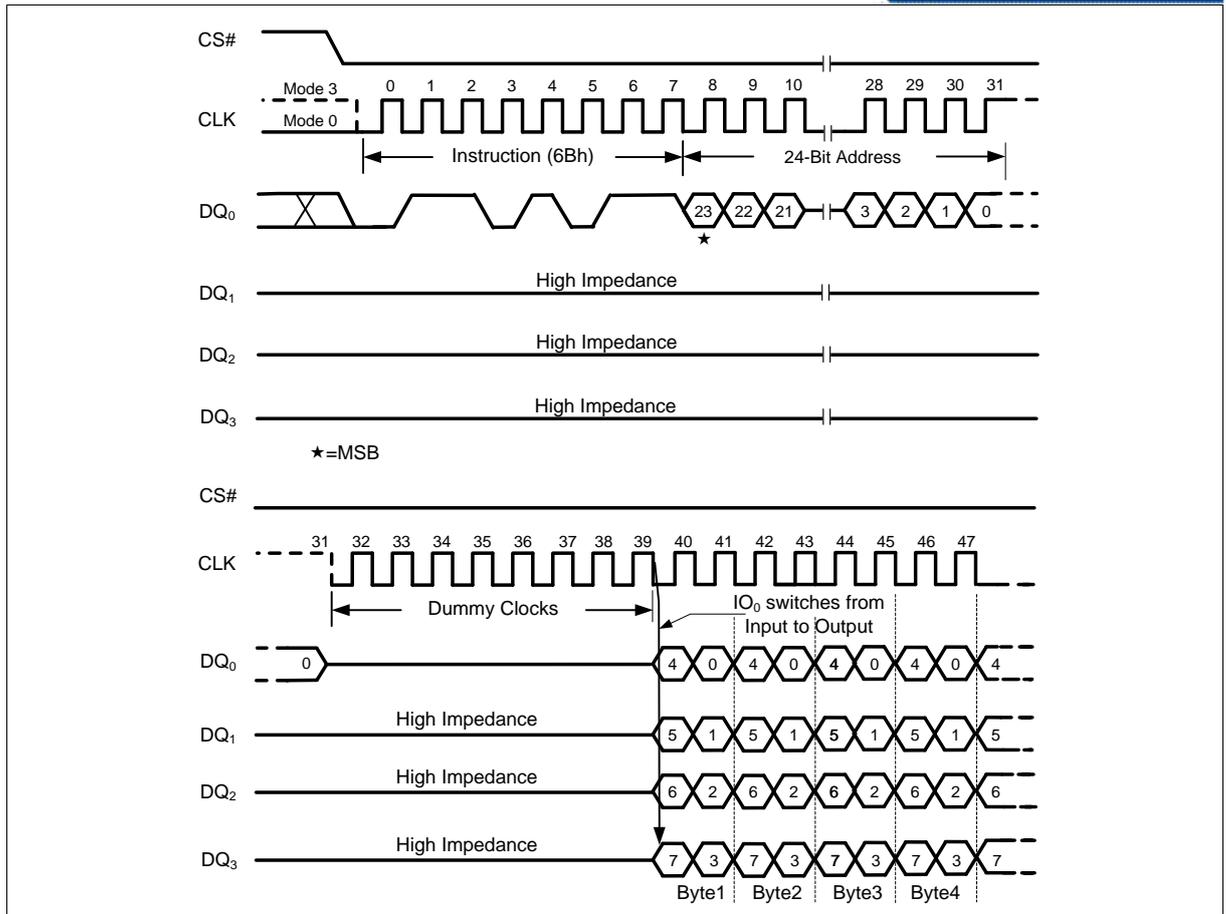
Figure 25 Fast Read Quad Output Instruction (SPI Mode only)

10.2.10. Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two I/O pins, DQ_0 and DQ_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits A23-A0 two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"
The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 26. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BBh instruction code, as shown in Figure 27. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on DQ_0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.
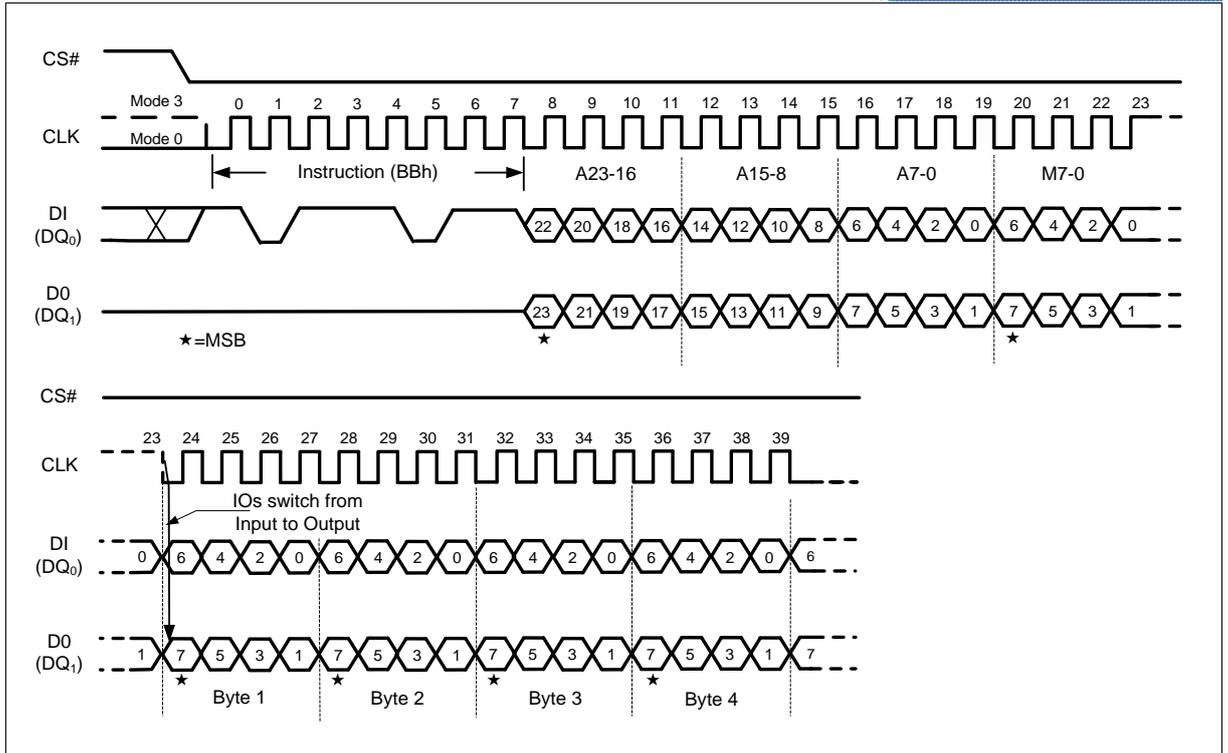
Figure 26 Fast Read Dual I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)
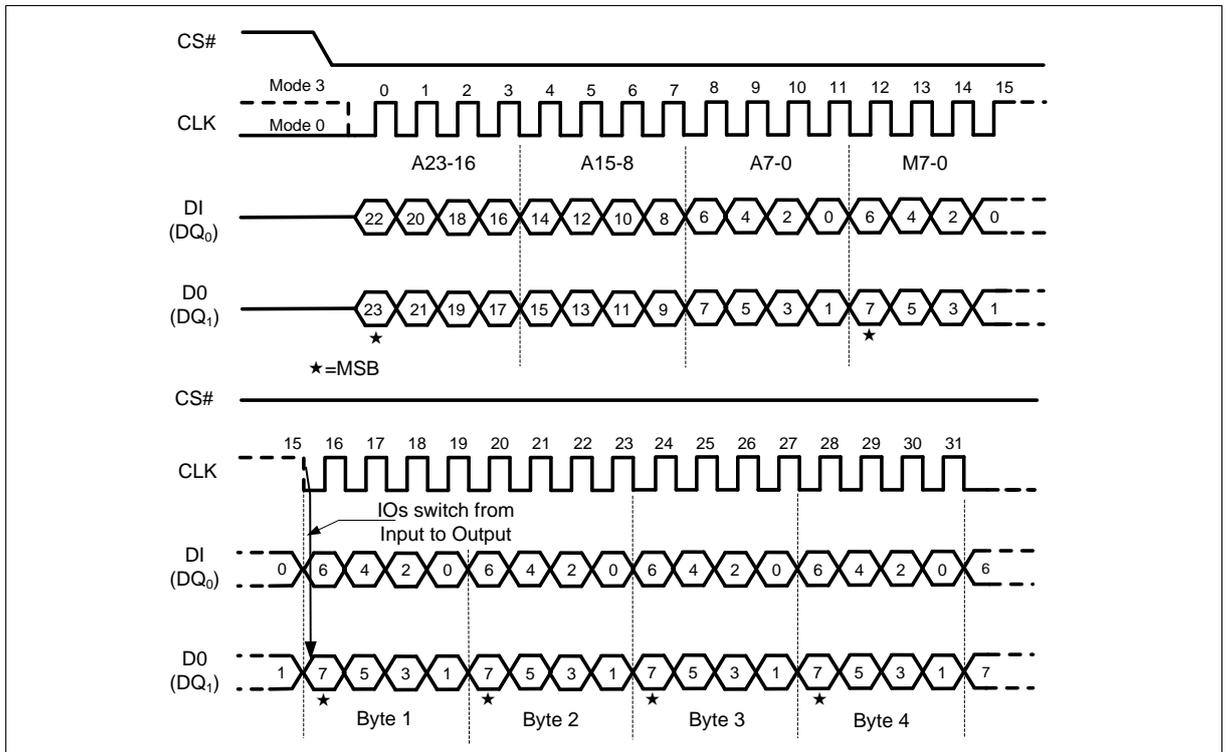

Figure 27 Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

10.2.11. Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins DQ_0, DQ_1, DQ_2 and DQ_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with "Continuous Read Mode"
TheFastReadQuadI/Oinstructioncanfurtherreduceinstructionoverheadthroughsettingthe"Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 28. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the EBh instruction code, as shown in Figure 29. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1, 0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next instruction (8 clocks), to ensure M4= 1 and return the device to normal operation.
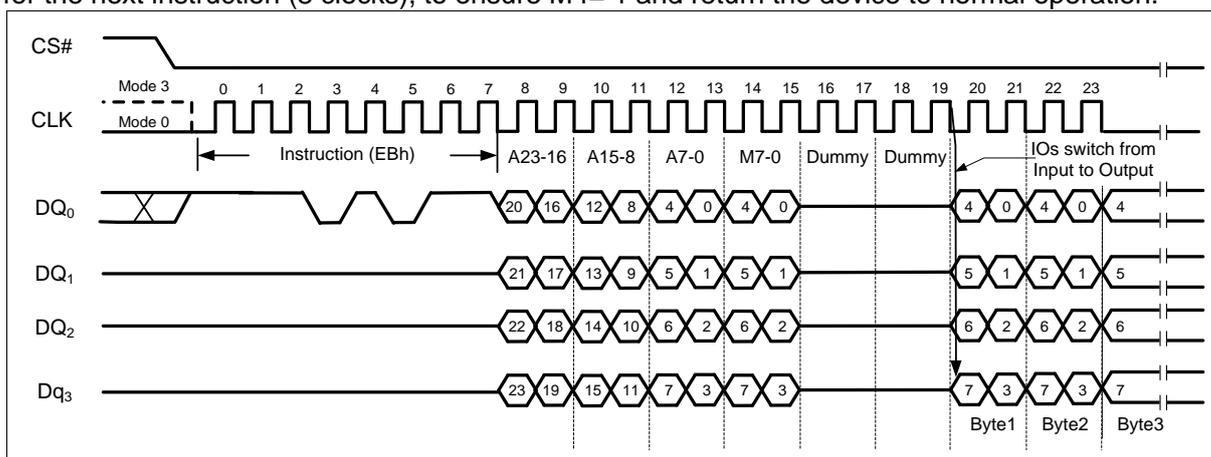
Figure 28 Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)
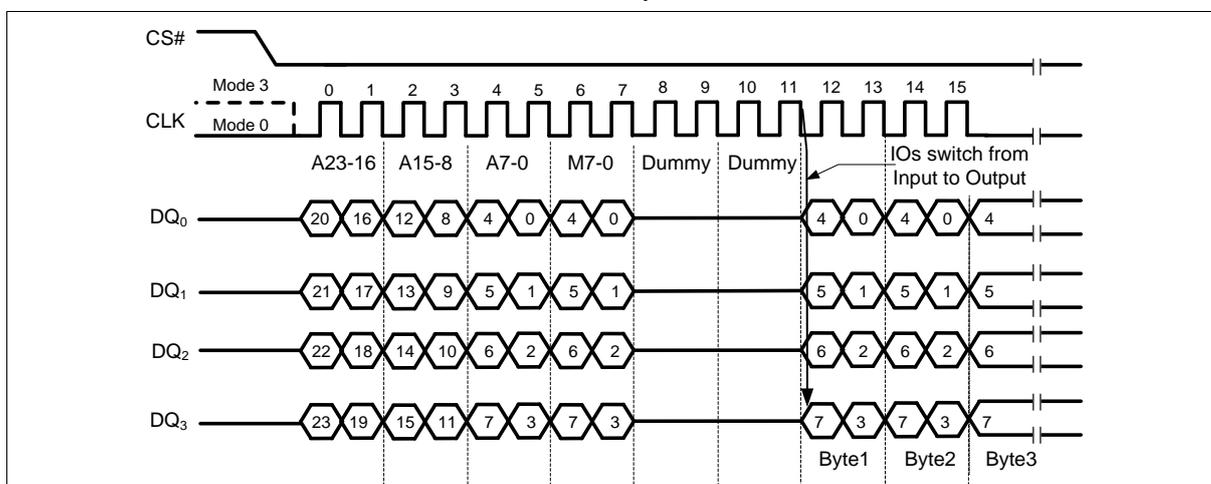
Figure 29 Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode
The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See "Set Burst with Wrap（77h）" for detail descriptions.

Fast Read Quad I/O (EBh) in QPI Mode
The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in Figure 30. When QPI mode is enabled, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 2.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages for details.

"Wrap Around" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages for details.
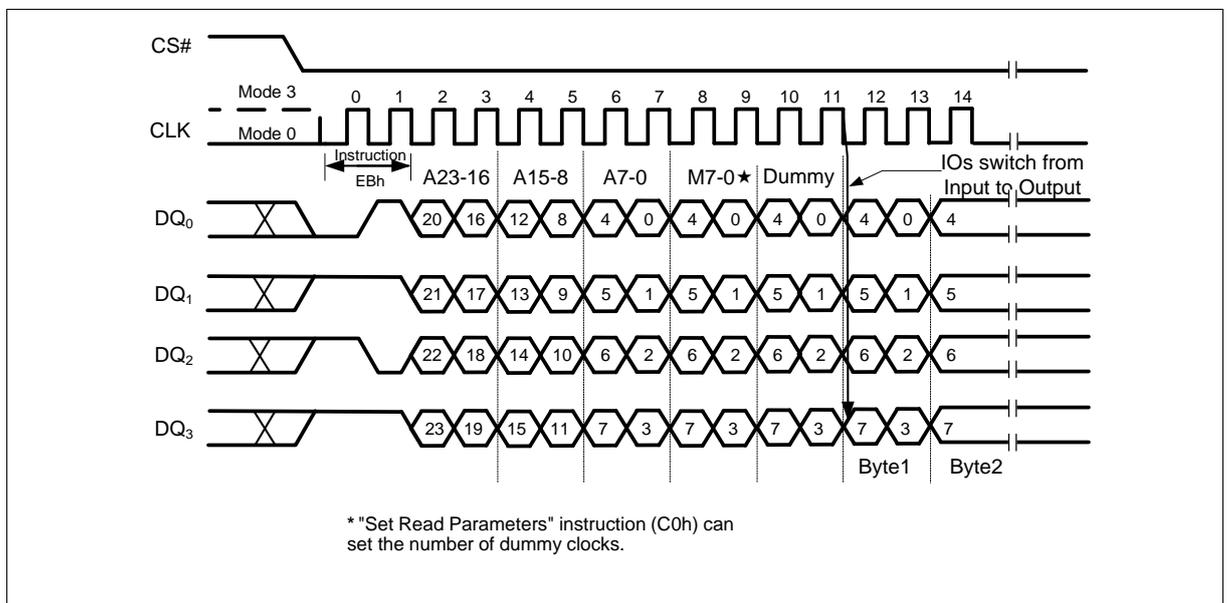
Figure 30 Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, QPI Mode)

10.2.12. DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Quad I/O (EBh) instructionexcept that the addressinput and the data output require DTR (Double Transfer Rate) operation. The address is latched on both rising and falling edge of CLK, and data shift out on both rising and falling edge of CLK. Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.10 Dummy clocks are required in SPI mode prior to the data output for EDh instruction. In QPI mode, the Dummy clocks can be configured by C0h instruction.
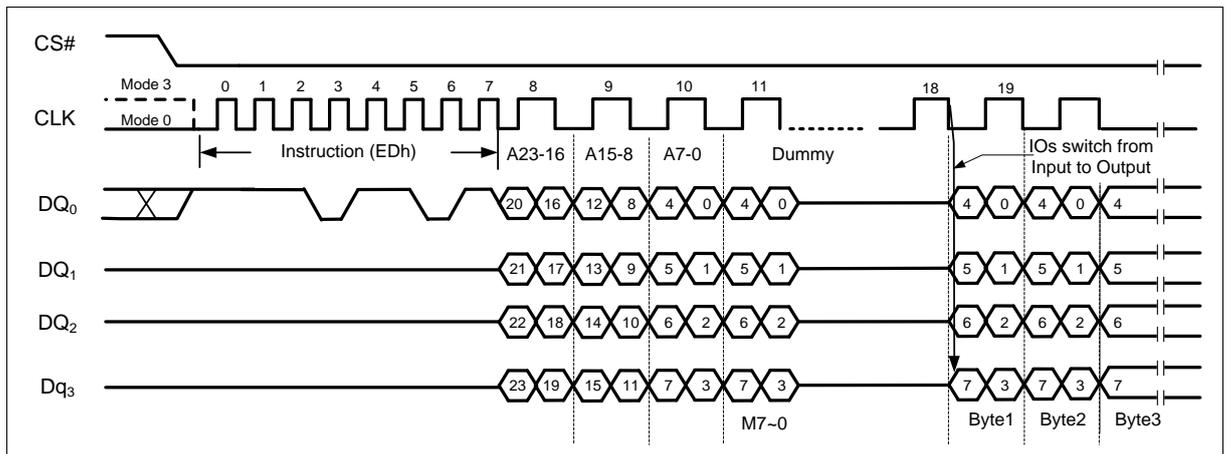
Figure 31 DTR Fast Read Quad I/O Instruction

Quad I/O DTR Read with "Continuous Read Mode"
The Quad I/O DTR Read command can further reduce command overhead through setting the "Continuous Read Mode"bits (M7-0) after the input address. If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O DTR Readcommand (after CS# is raised and then lowered) does not require the EDH command code. If the "Continuous Read Mode"bits (M5-4) do not equal to (1, 0), the next command requires the first EDH command code, thus returning to normaloperation. The only way to quit the Quad I/O DTR Continuous Read Mode" is to set the "Continuous Read Mode" bits (M5-4) not equal to (1, 0).
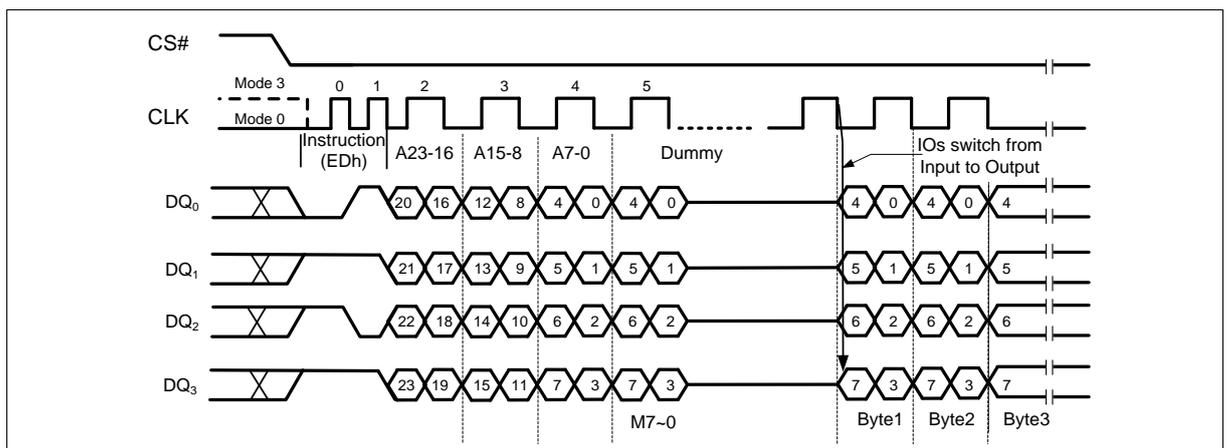
Figure 32 DTR Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, QPI Mode)
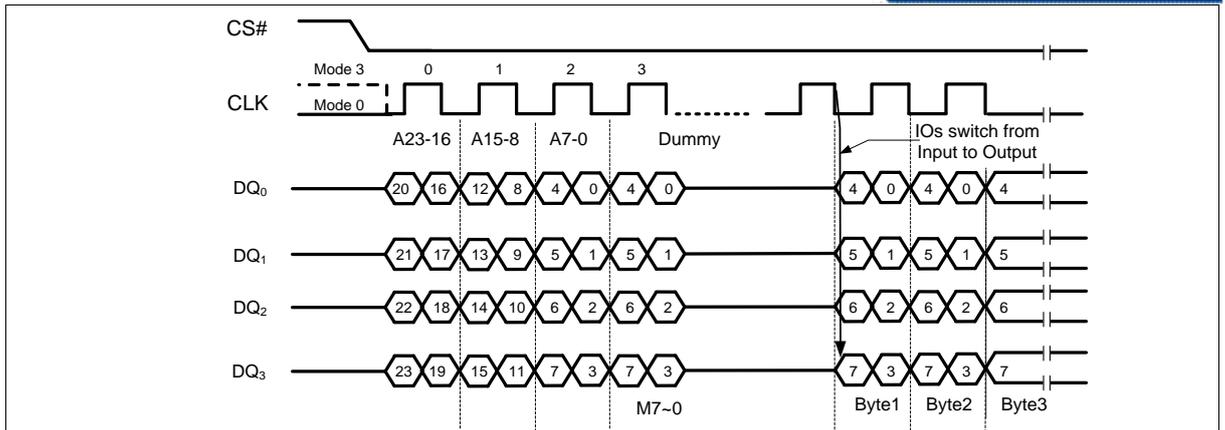
Figure 33 Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

10.2.13. Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) instruction is used in conjunction with "Fast Read Quad I/O" instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the CS# pin low and then shifting the instruction code "77h" followed by 24 dummy bits and 8 "Wrap Bits", W7-0. The instruction sequence is shown in Figure 31. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
00	Yes	8-byte	No	N/A
01	Yes	16-byte	No	N/A
10	Yes	32-byte	No	N/A
11	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following "Fast Read Quad I/O" instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction to reset W4 = 1 prior to any normal Read instructions since FM25LQ128I3 does not have a hardware Reset Pin.
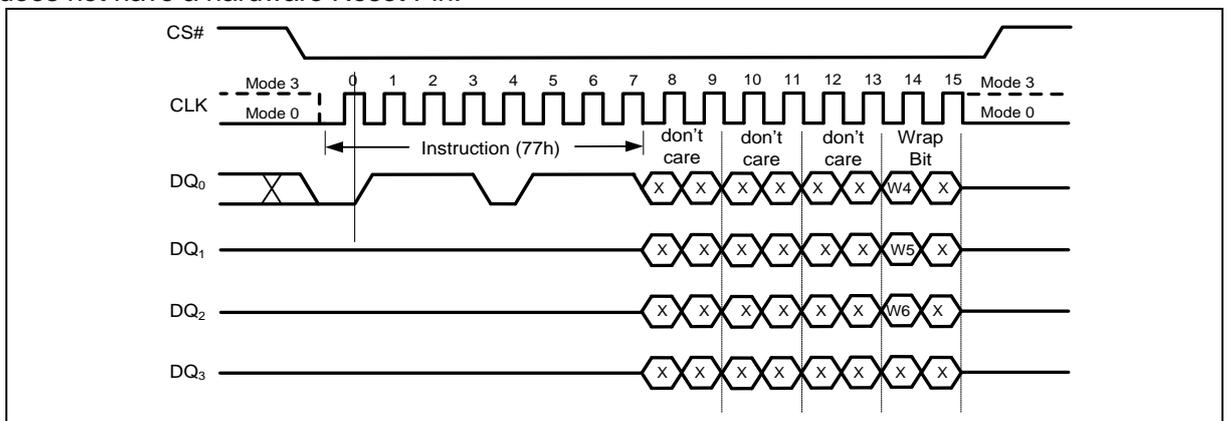
Figure 31 Set Burst with Wrap Instruction for SPI Mode

10.2.14. Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased(FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code "02h" followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 32 and Figure 33.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of t_{PP} (See "11.6AC Electrical Characteristics"). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks.
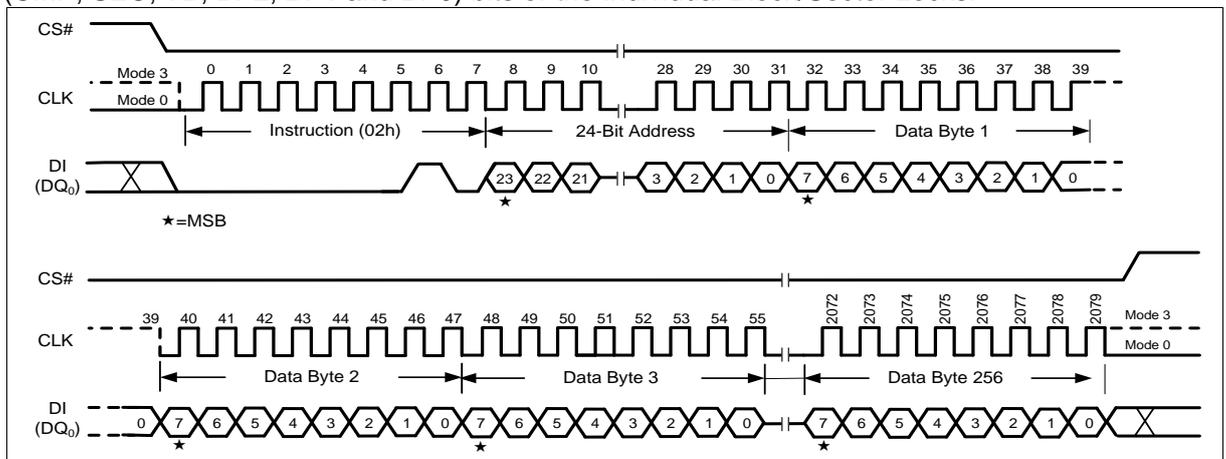

**Figure 32 Page Program Instruction (SPI Mode)**
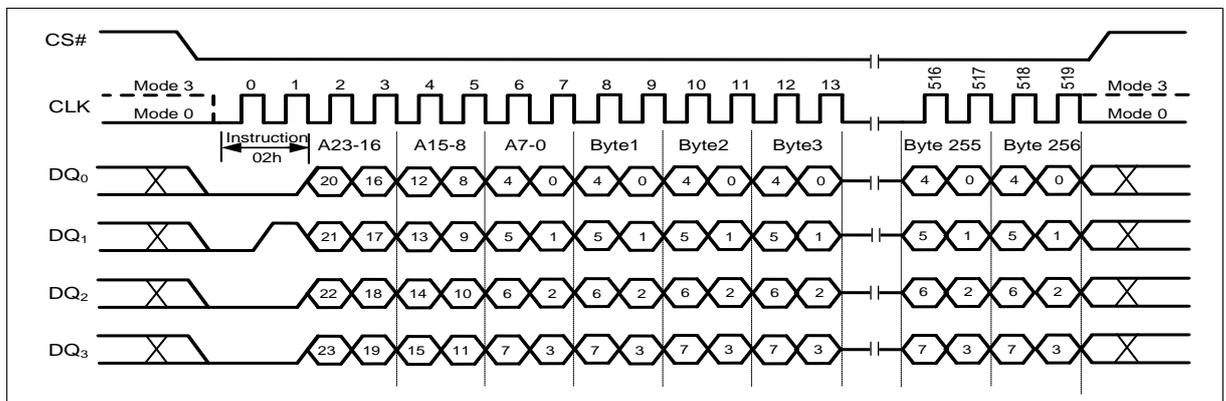
Figure 33 Page Program Instruction (QPI Mode)

10.2.15. Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: DQ_0, DQ_1, DQ_2, and DQ_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the CS# pin low then shifting the instruction code "32h" followed by a 24-bit address A23-A0 and at least one data byte, into the DQ pins. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The QuadPage Program instruction sequence is shown in Figure 34.
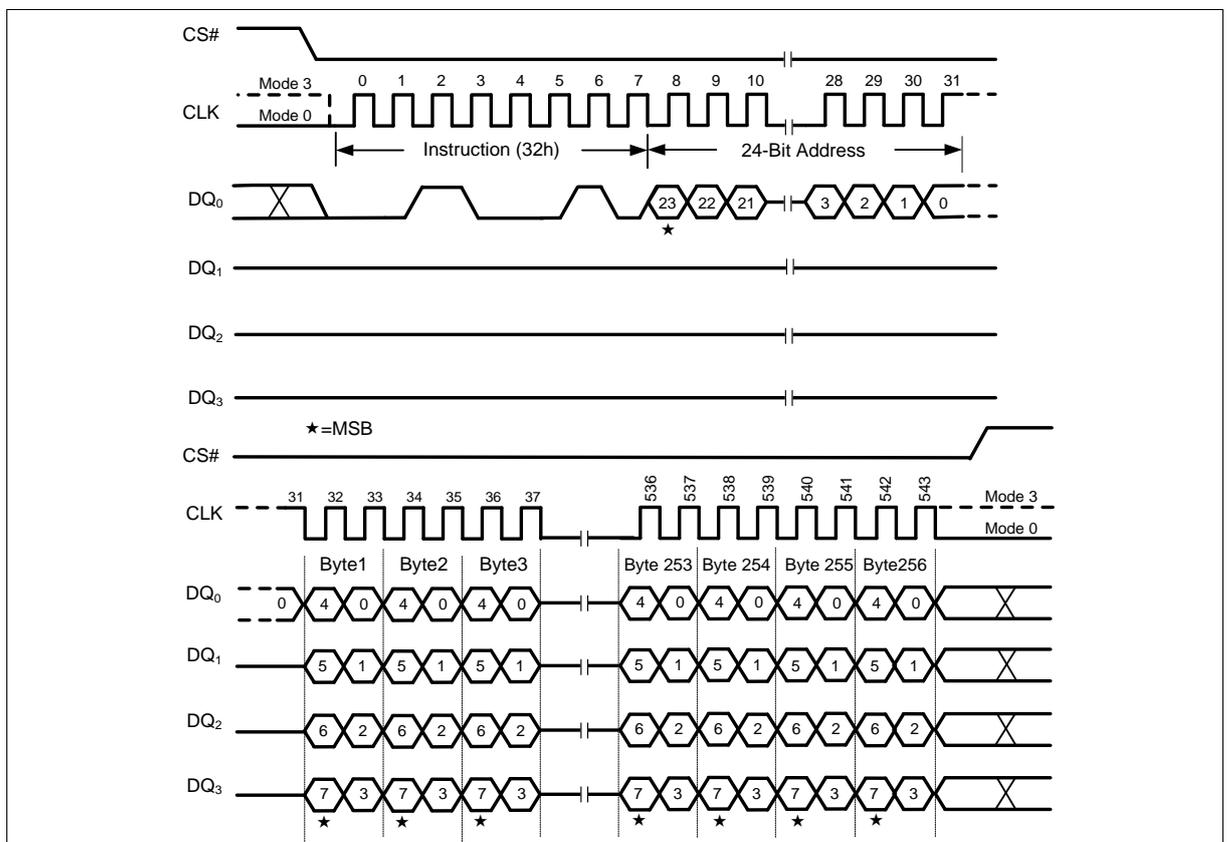
Figure 34 Quad Input Page Program Instruction (SPI Mode only)

10.2.16. Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "20h" followed a 24-bit sector address A23-A0 (see Figure 4). The Sector Erase instruction sequence is shown in Figure 35&Figure 36.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See "11.6AC Electrical Characteristics"). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks (see Table 4Status Register Memory Protection table).
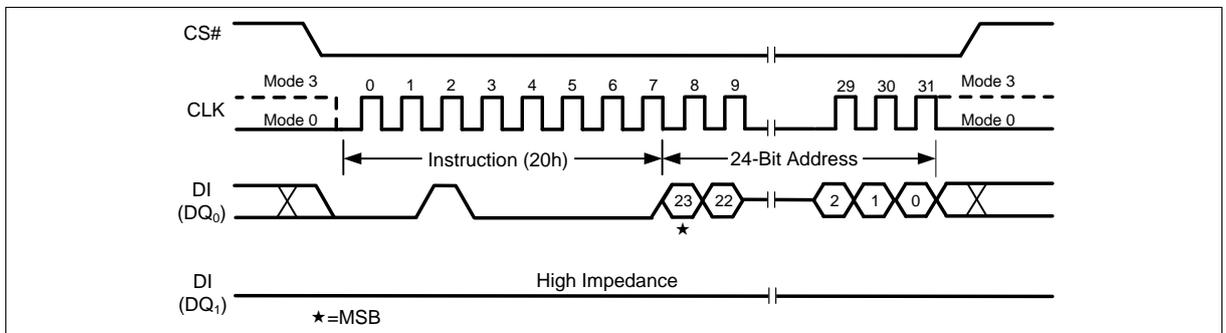
**Figure 35 Sector Erase Instruction (SPI Mode)**
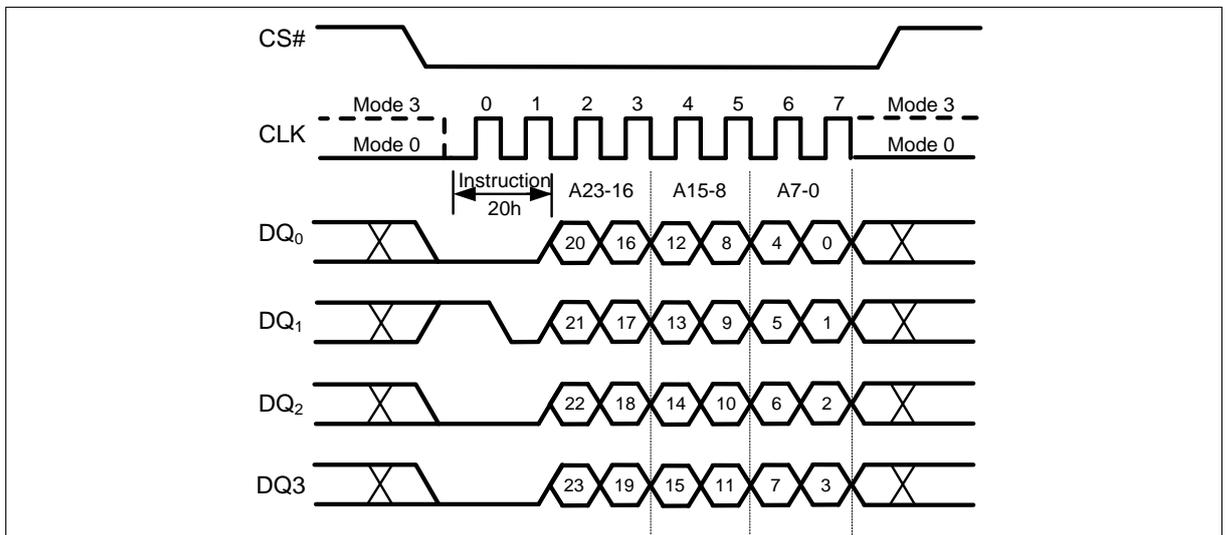
Figure 36 Sector Erase Instruction (QPI Mode)

10.2.17. 32KB Block Erase (BE32) (52h)

The 32KB Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shiftingthe instructioncode"52h"followeda24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 37&Figure 38.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE1} (See "11.6AC Electrical Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks.
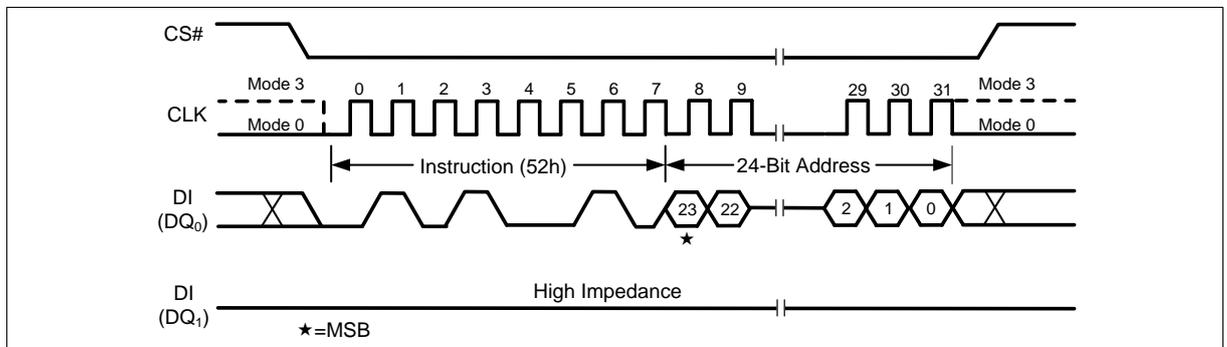
**Figure 37 32KB Block Erase Instruction (SPI Mode)**
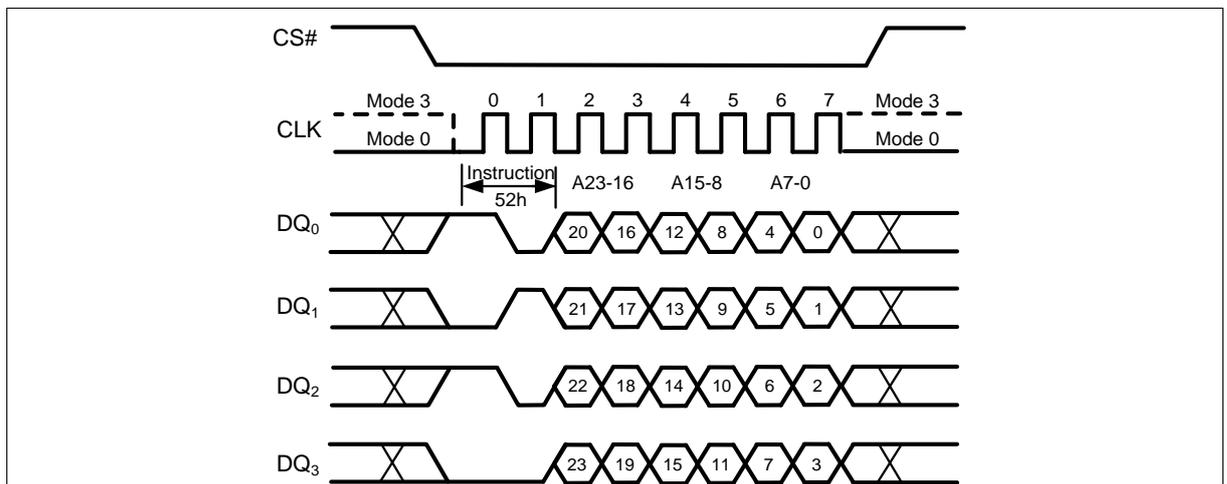
Figure 38 32KB Block Erase Instruction (QPI Mode)

10.2.18. 64KB Block Erase (BE) (D8h)

The 64KB Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "D8h" followed a 24-bit block address A23-A0. The Block Erase instruction sequence is shown in Figure 39&Figure 40.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See 11.6AC Electrical Characteristics"). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks.
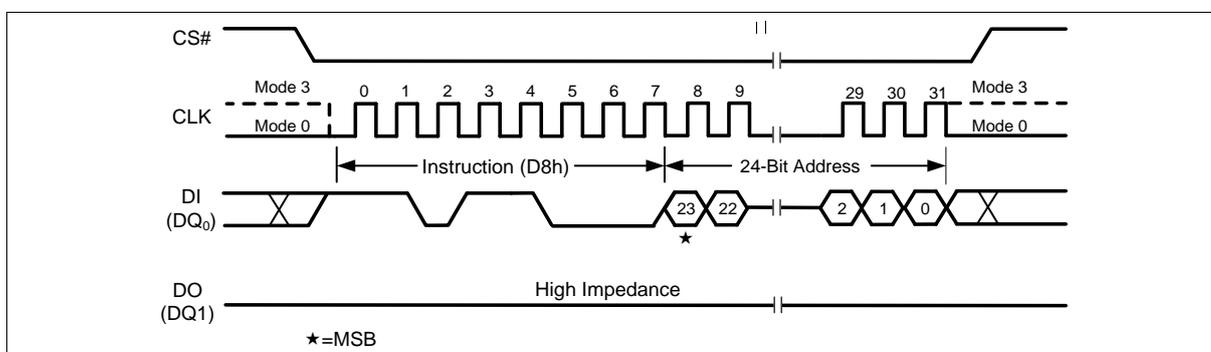
**Figure 39 64KB Block Erase Instruction (SPI Mode)**
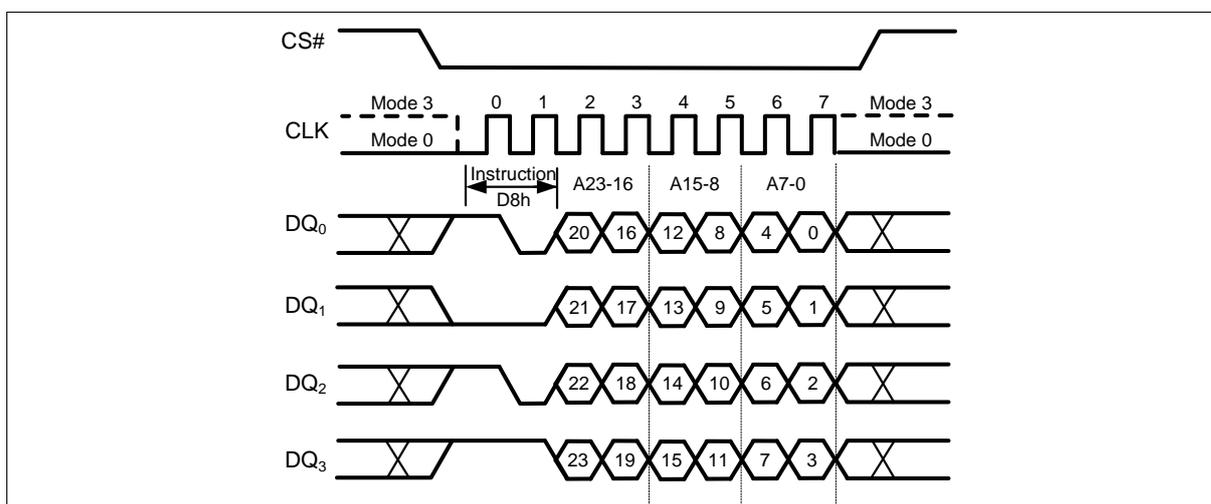
Figure 40 64KB Block Erase Instruction (QPI Mode)

10.2.19. Chip Erase (CE) (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "C7h" or "60h". The Chip Erase instruction sequence is shown in Figure 41.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instructionwill not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See "11.6AC Electrical Characteristics"). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits or the Individual Block/Sector Locks.
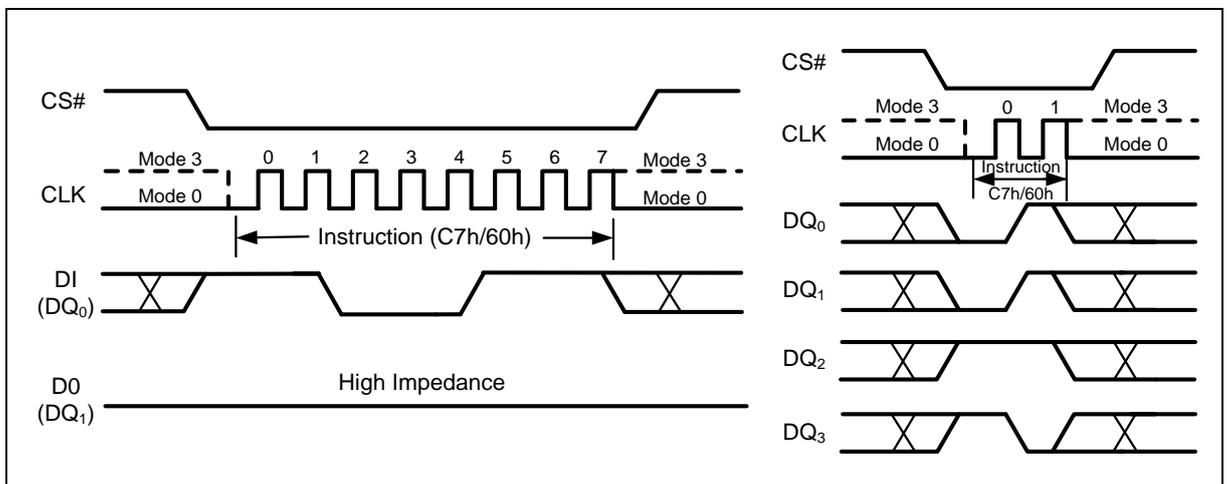

Figure 41 Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)

10.2.20. Erase / Program Suspend (75h)

The Erase/Program Suspend instruction "75h", allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read data from any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 42&Figure 43.

The Write Status Register instruction (01h, 31h), Program and Erase instructionsare not allowed during Program/Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Suspend instruction is ignored.

The Erase/Program Suspend instruction "75h" will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the WIP bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the WIP bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of "t_{SUS}" (See"11.6AC Electrical Characteristics") is required to suspend the erase or program operation. The WIP bit in the Status Register will be cleared from 1 to0 within "t_{SUS}" and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction "75h" is not issued earlier than a minimum of time of "t_{SUS}" following the preceding Resume instruction "7Ah".

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.
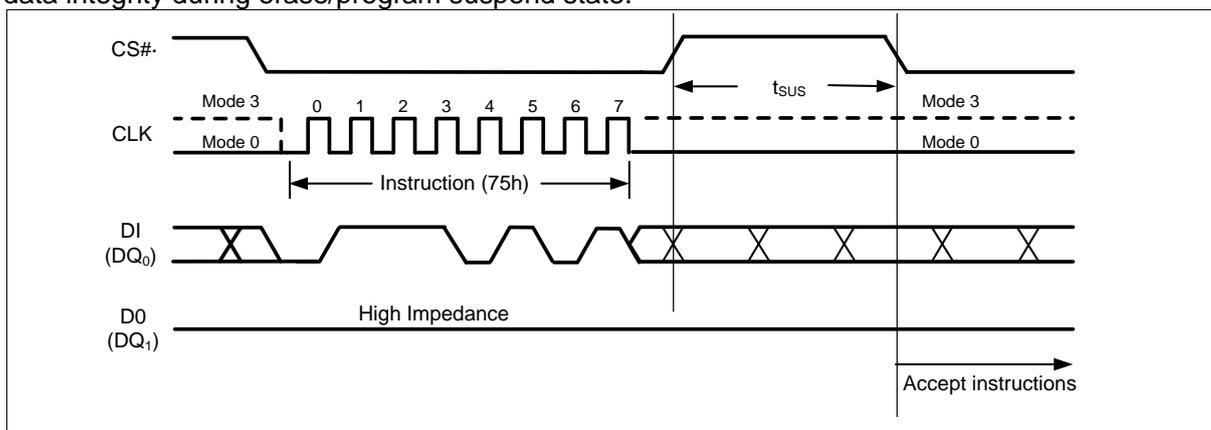

**Figure 42 Erase/Program Suspend Instruction (SPI Mode)**
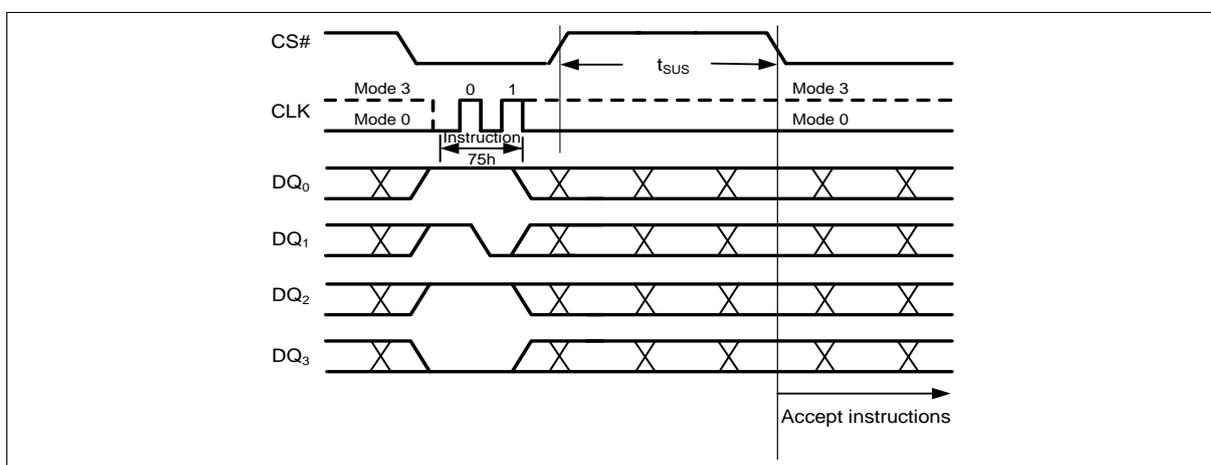
Figure 43 Erase/Program Suspend Instruction (QPI Mode)

10.2.21. Erase / Program Resume (7Ah)

The Erase/Program Resume instruction "7Ah" must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction "7Ah" will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume instruction "7Ah" will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 44&Figure 45.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of "t_{SUS}" following a previous Resume instruction.
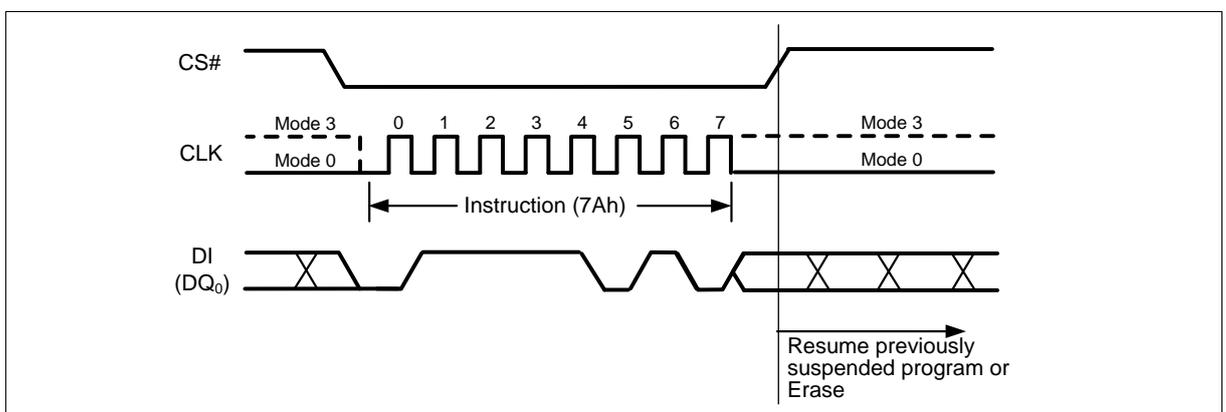

**Figure 44 Erase/Program Resume Instruction (SPI Mode)**
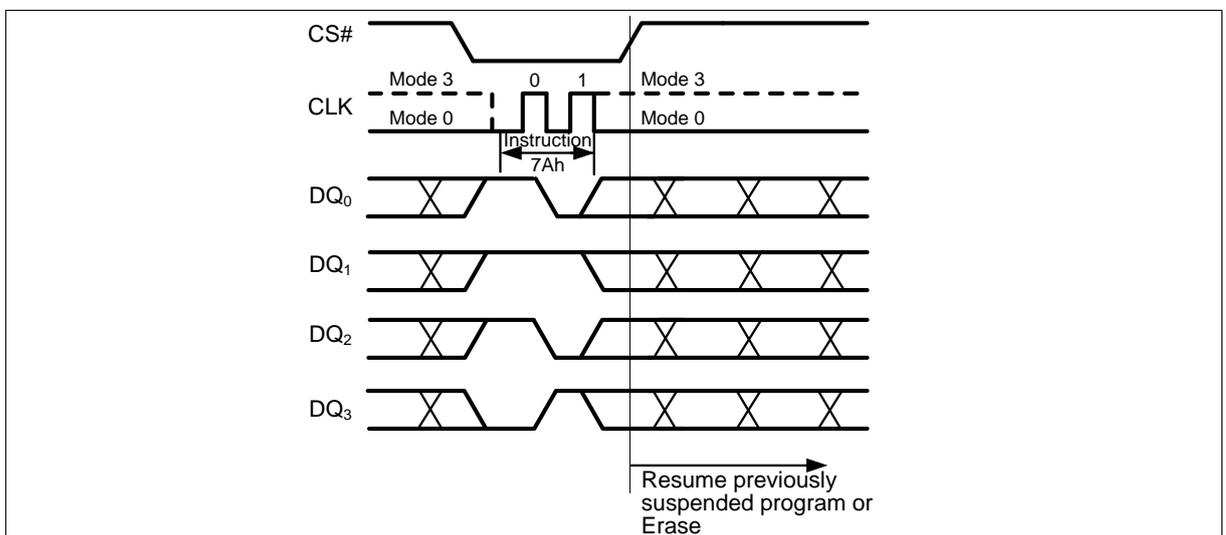
Figure 45 Erase/Program Resume Instruction (QPI Mode)

10.2.22. Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See I_{CC1} and I_{CC2} in"11.4DC Electrical Characteristics"). The instruction is initiated by driving the CS# pin low and shifting the instruction code "B9h" as shown in Figure 46&Figure 47.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See "11.6AC Electrical Characteristics"). While in the power-down state only the Release from Power- down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.
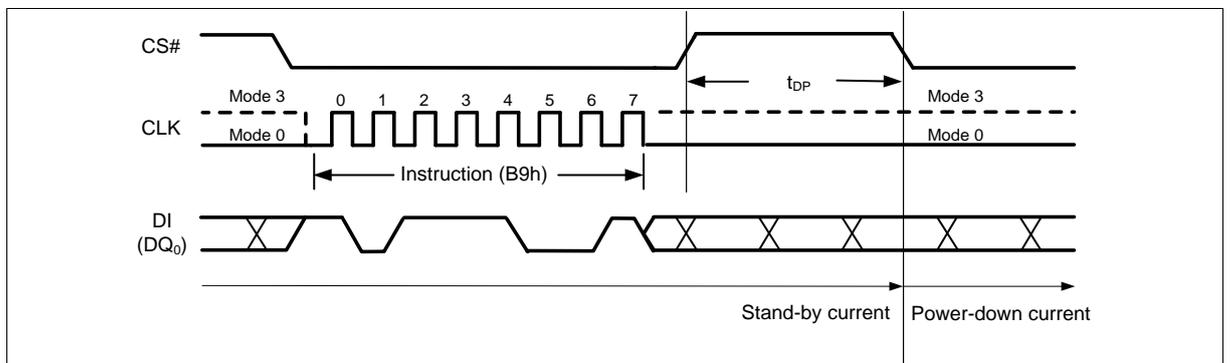

**Figure 46 Deep Power-down Instruction (SPI Mode)**
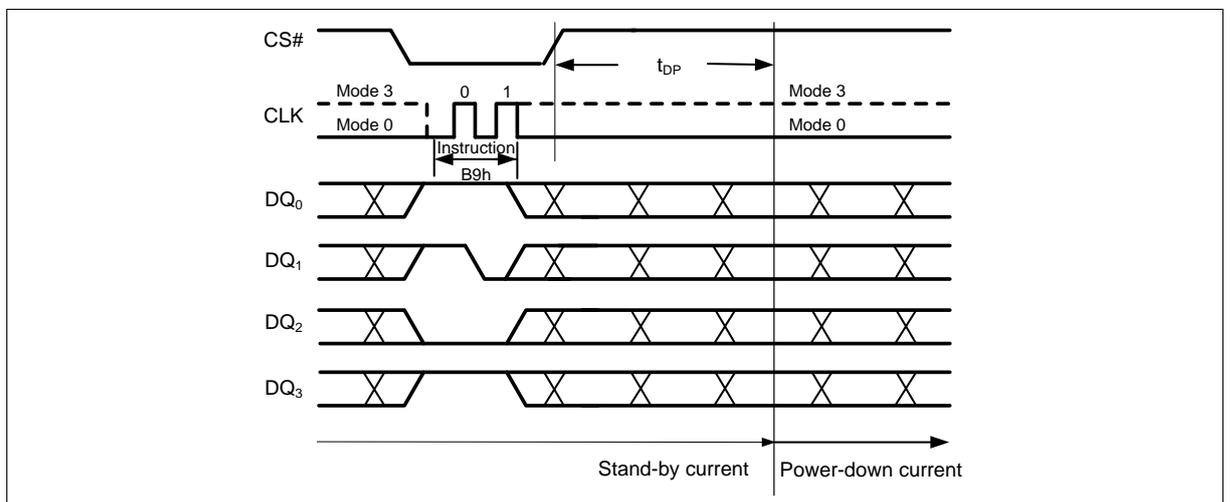
Figure 47 Deep Power-down Instruction (QPI Mode)

10.2.23. Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high as shown in Figure 48&Figure 49. Release from power-down will take the time duration of t_{RES1} (See "11.6AC Electrical Characteristics") before the device will resume normal operation and other instructions are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown inFigure 50&Figure 51. The Device ID value for the FM25LQ128I3 is listed in Table 6Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 50&Figure 51, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See "11.6AC Electrical Characteristics"). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equals1) the instruction is ignored and will not have any effect on the current cycle.
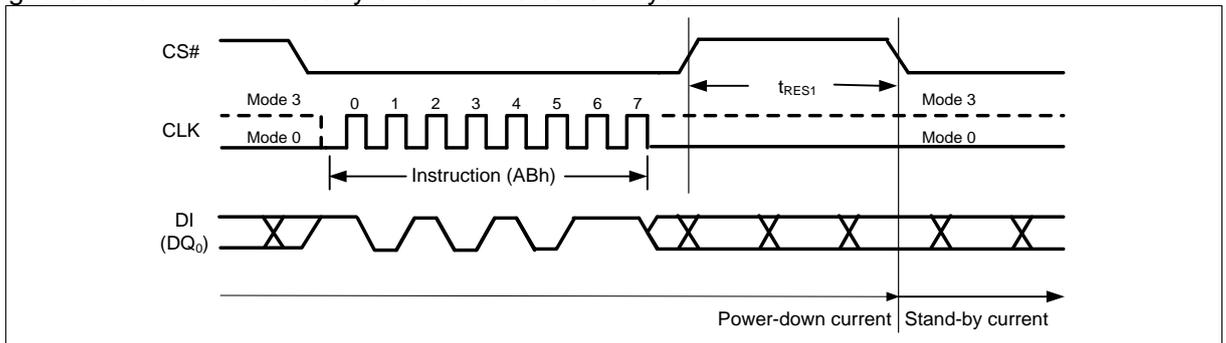

**Figure 48 Release Power-down Instruction (SPI Mode)**
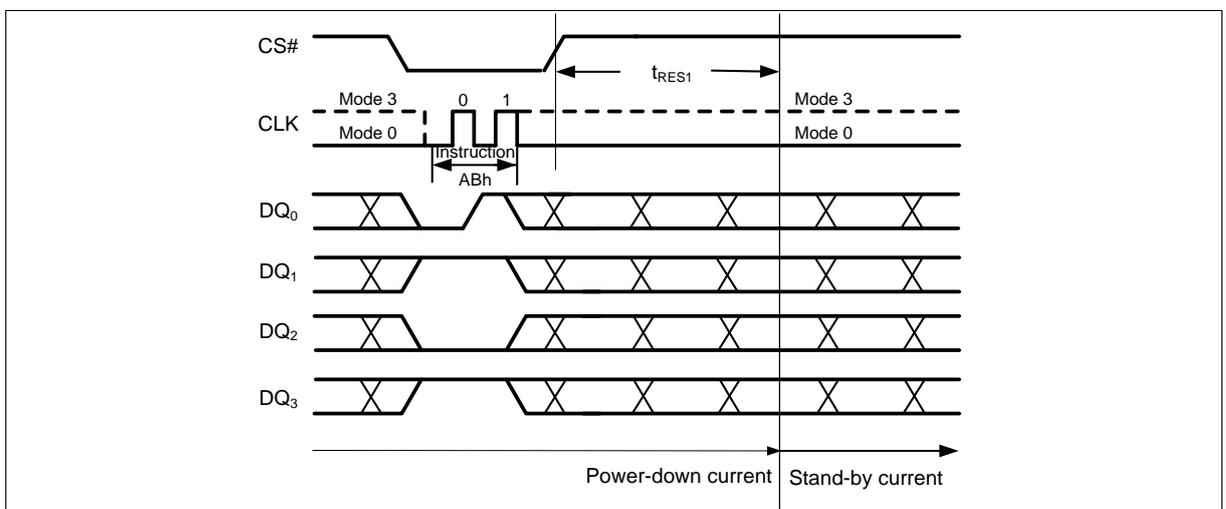
**Figure 49 Release Power-down Instruction (QPI Mode)**
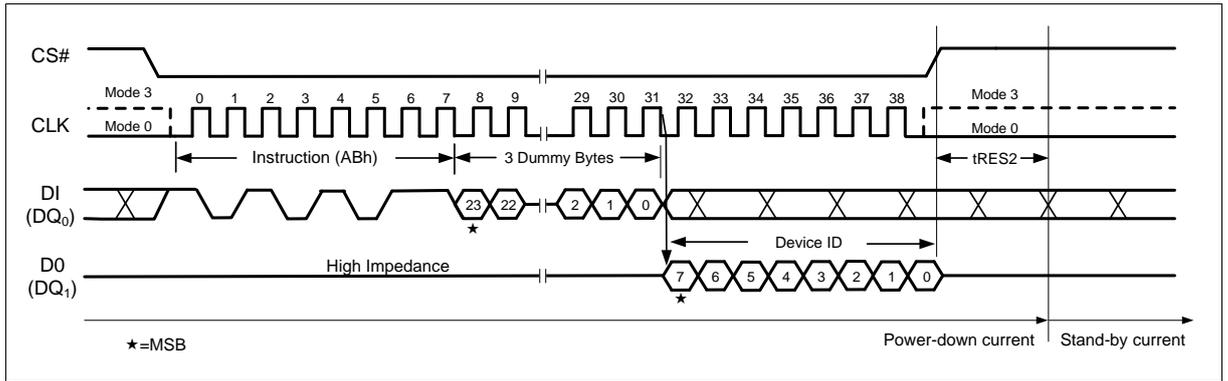
Figure 50 Release Power-down / Device ID Instruction (SPI Mode)
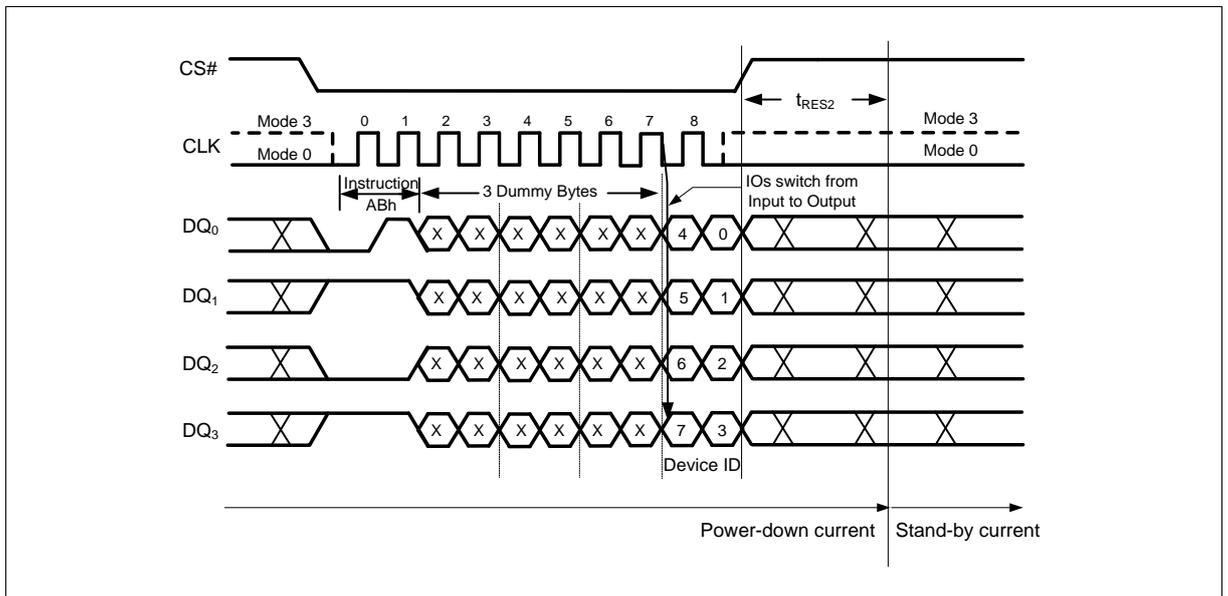

Figure 51 Release Power-down / Device ID Instruction (QPI Mode)

10.2.24. Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / DeviceID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "90h" followed by a 24-bit address A23-A0 of 000000h. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 52&Figure 53. The Device ID value for the FM25LQ128I3 is listed in Table 6Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.
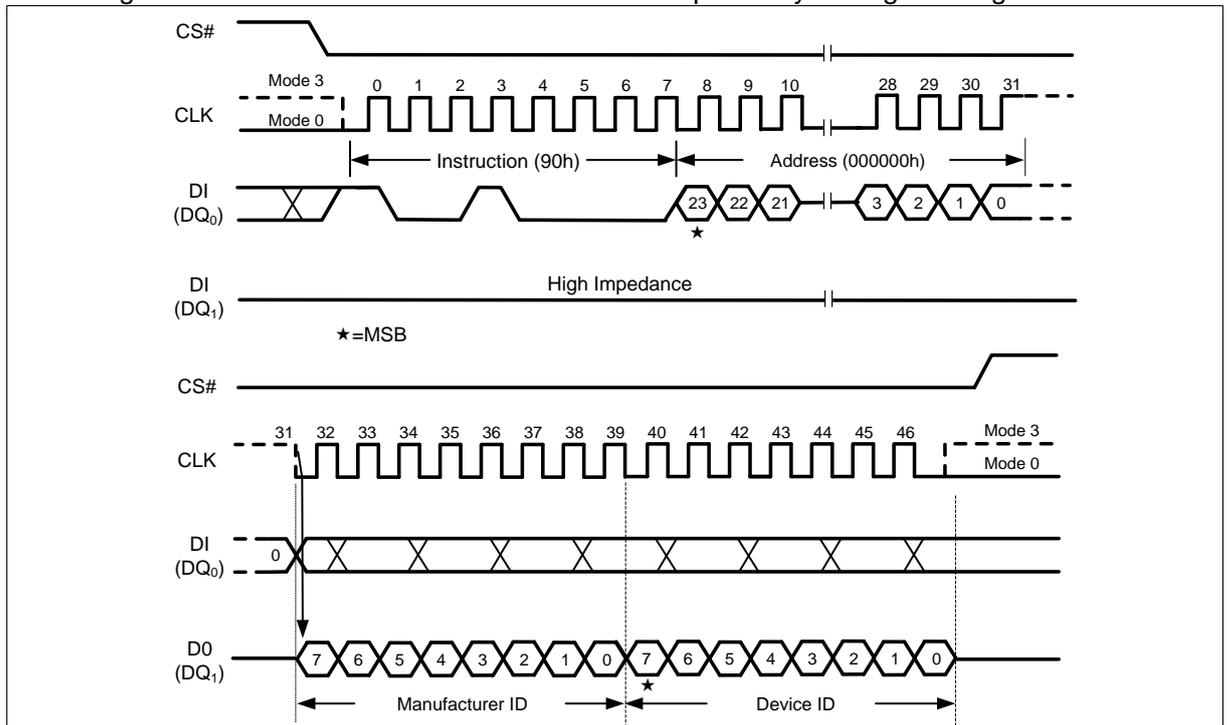
Figure 52 Read Manufacturer / Device ID Instruction (SPI Mode)
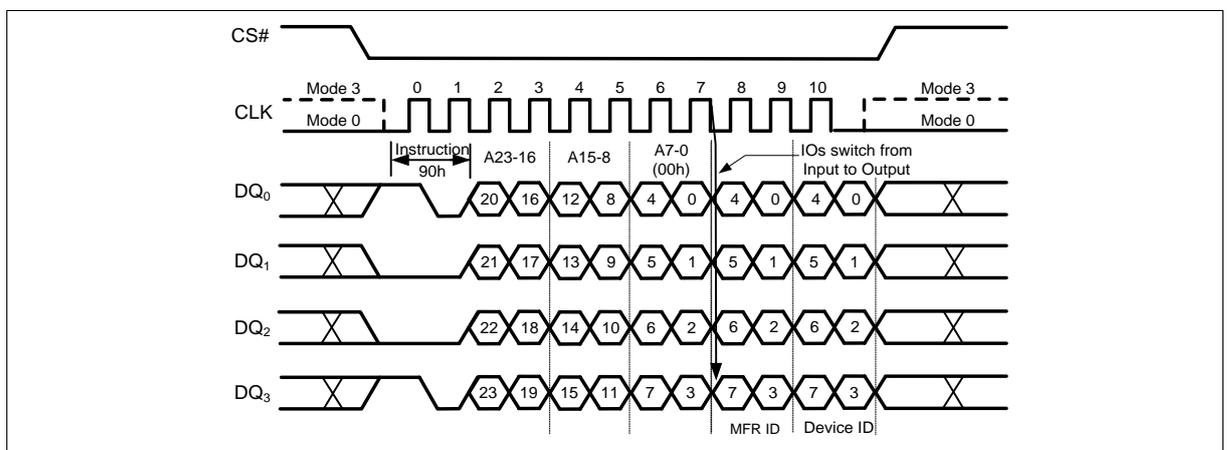
Figure 53 Read Manufacturer / Device ID Instruction (QPI Mode)

10.2.25. Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "92h" followed by a24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits, with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 54. The Device ID value for the FM25LQ128I3 is listed in Table 6Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.
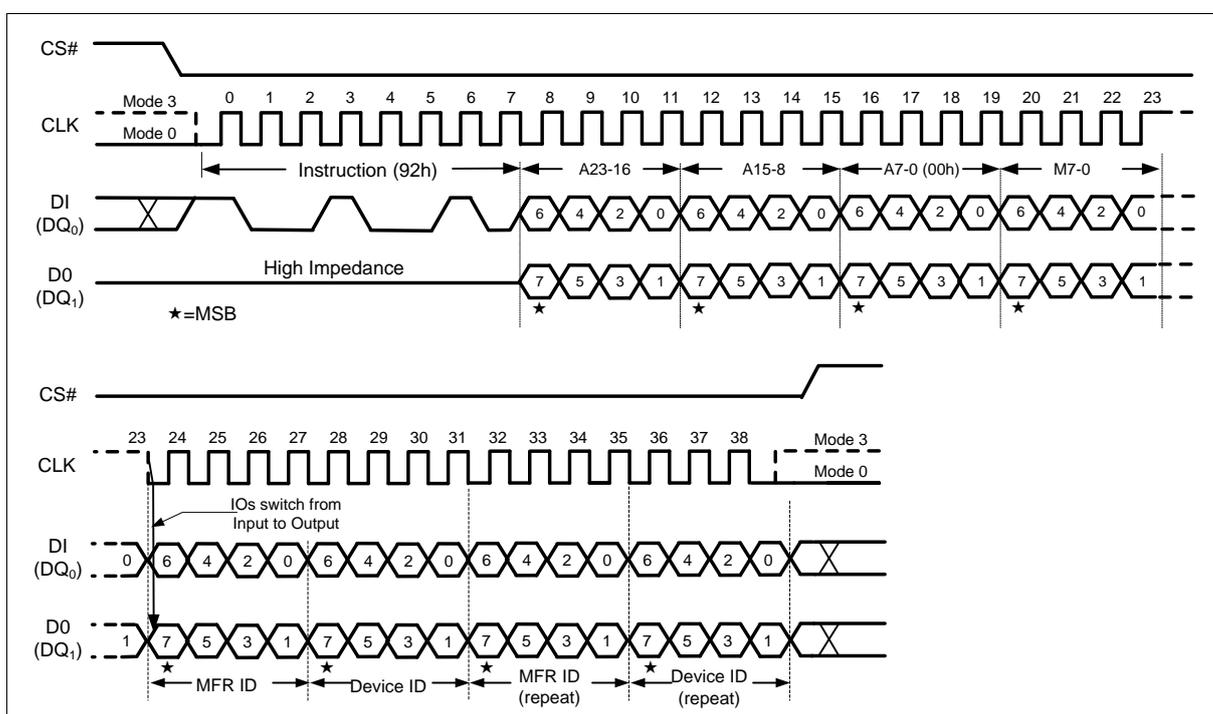

Figure 54 Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)

Note:
The "Continuous Read Mode" bits M7-M0 must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

10.2.26. Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "94h" followed by a 24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits and then four clock dummy cycles, with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 55. The Device ID value for the FM25LQ128I3 is listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.
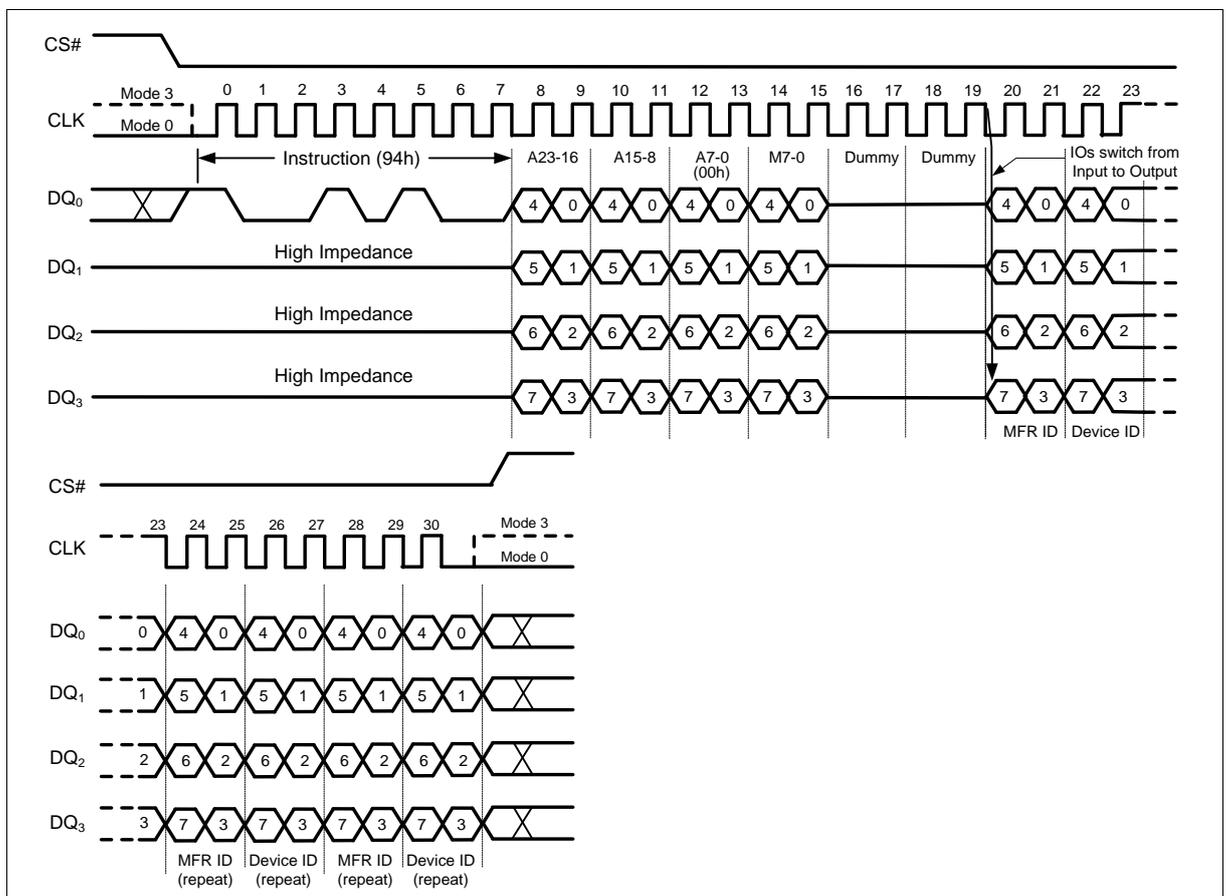

Figure 55 Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

Note:
The "Continuous Read Mode" bits M7-M0 must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

10.2.27. Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each FM25LQ128I3 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code "4Bh" followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 56.
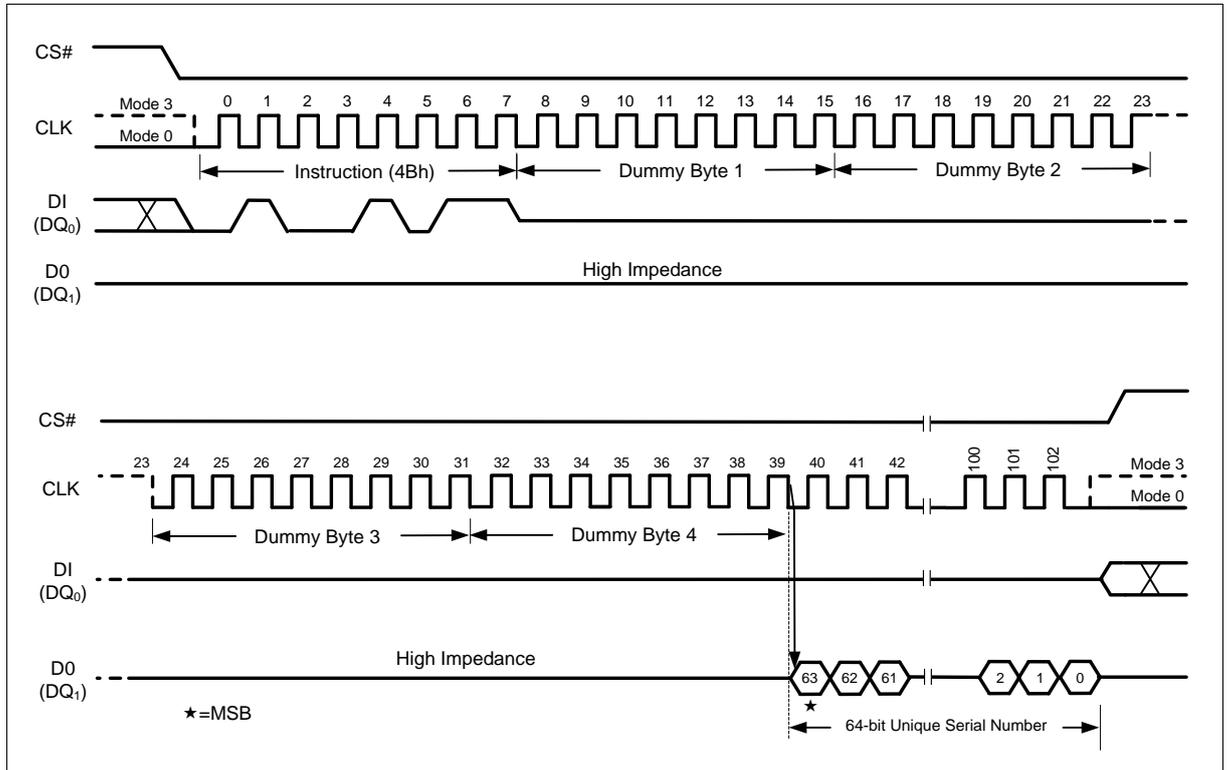
Figure 56 Read Unique ID Number Instruction (SPI Mode only)

10.2.28. Read JEDEC ID (9Fh)

For compatibility reasons, the FM25LQ128I3 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories. The instruction is initiated by driving the CS# pin low and shifting the instruction code "9Fh". The JEDEC assigned Manufacturer ID byte for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity ID7-ID0 are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 57&Figure 58. For memory type and capacity values refer to Table 6Manufacturer and Device Identification table.
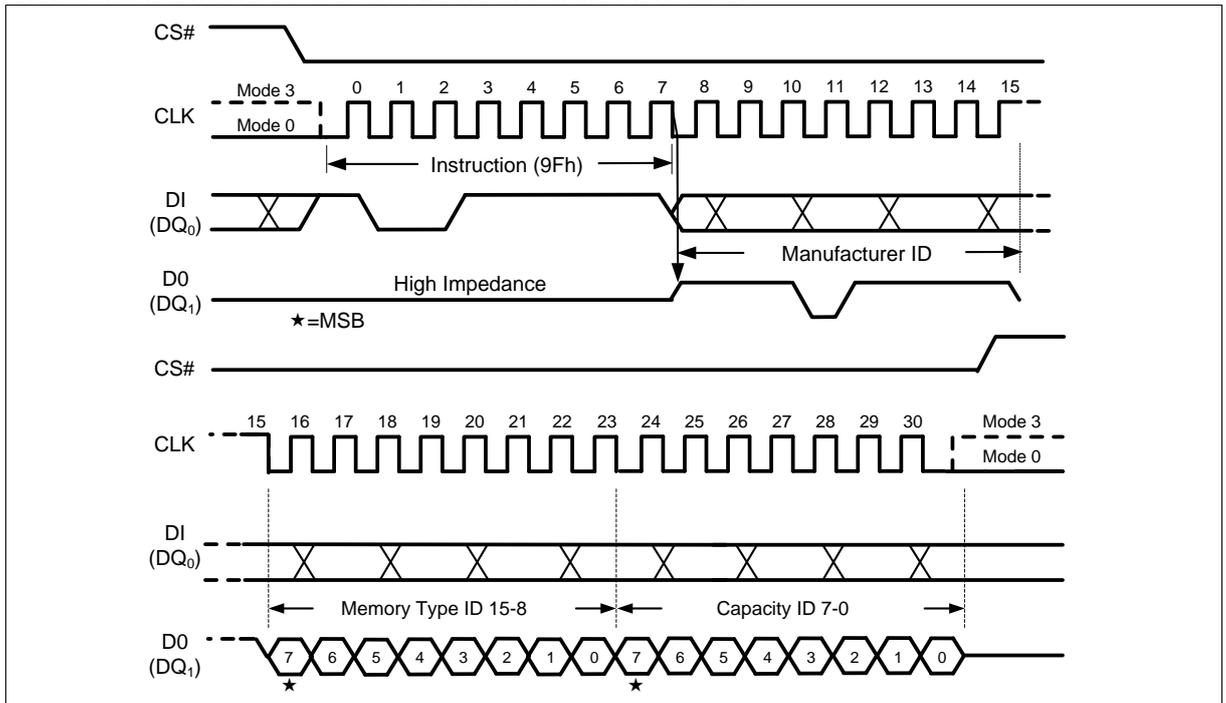
Figure 57 Read JEDEC ID Instruction (SPI Mode)
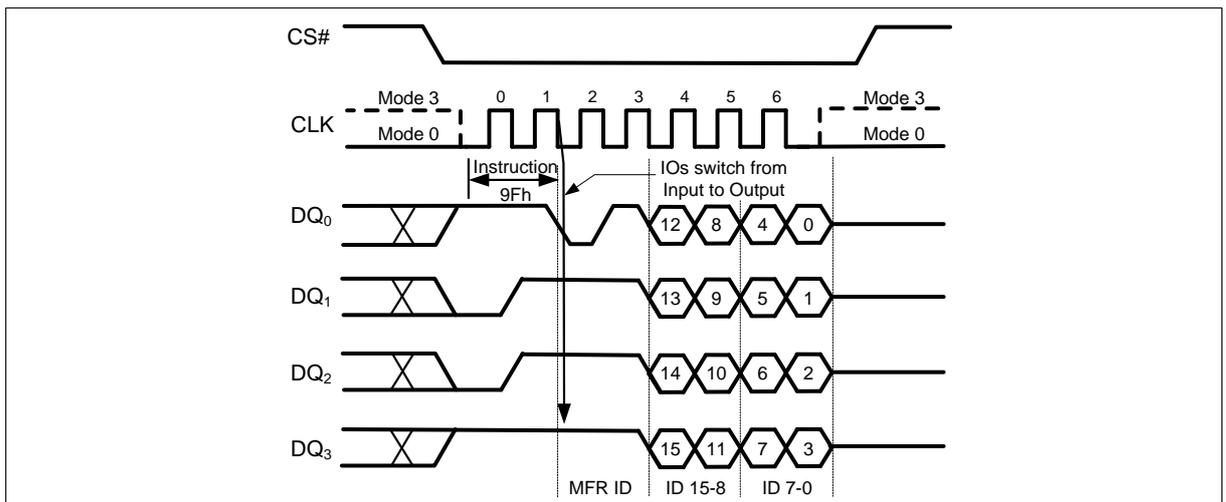
Figure 58 Read JEDEC ID Instruction (QPI Mode)

10.2.29. Read SFDP Register(5Ah)

The FM25LQ128I3 features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The concept of SFDP is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216B.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0) [1] into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown inFigure 59. For SFDP register values and descriptions, refer to the following SFDP Definition table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.
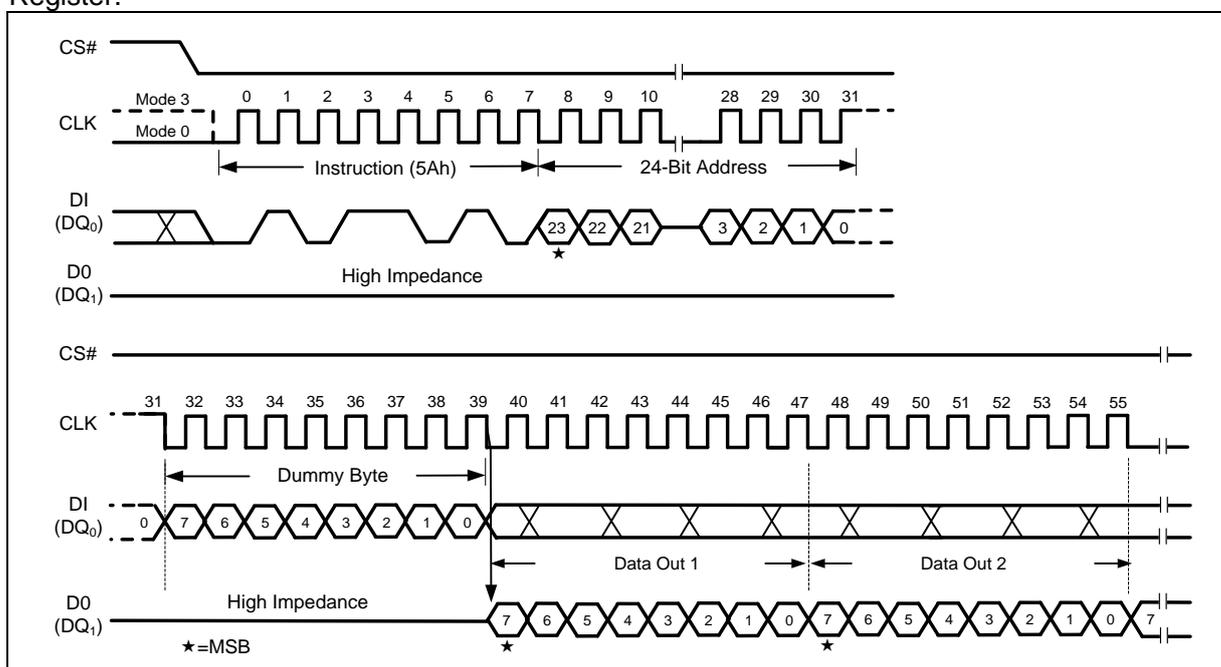
Figure 59 Read SFDP Register Instruction

Serial Flash Discoverable Parameter (JEDEC) Definition Table

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
00h	53h	SFDP Signature	SFDP Signature = 50444653h
01h	46h	SFDP Signature	
02h	44h	SFDP Signature	
03h	50h	SFDP Signature	
04h	06h	SFDP Minor Revision Number	JESD216B
05h	01h	SFDP Major Revision Number	
06h	01h	Number of Parameter Headers (NPH)	2 Parameter Header
07h	FFh	Reserved	
08h	00h	PID[3](0): ID Number	00h=JEDEC specified
09h	06h	PID(0): Parameter Table Minor Revision Number	JESD216B
0Ah	01h	PID(0): Parameter Table Major Revision Number	
0Bh	10h	PID(0): Parameter Table Length	16Dwords[2]

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
0Ch	30h	PID(0): Parameter Table Pointer (PTP) (A7-A0)	PID(0) Pointer = 000030h
0Dh	00h	PID(0): Parameter Table Pointer (PTP) (A15-A8)	
0Eh	00h	PID(0): Parameter Table Pointer (PTP) (A23-A16)	
0Fh	FFh	Reserved	
10h	A1h	PID(1):ID Number	FMSH manufacture ID
11h	00h	PID(1): Parameter Table Minor Revision Number	Version 1.0
12h	01h	PID(1): Parameter Table Major Revision Number	
13h	03h	PID(1): Parameter Table Length	4Dwords
14h	90h	PID(1): Parameter Table Pointer (PTP) (A7-A0)	PID(1) Pointer =
15h	00h	PID(1): Parameter Table Pointer (PTP) (A15-A8)	000090h
16h	00h	PID(1): Parameter Table Pointer (PTP) (A23-A16)	
17h	FFh	Contains 0xFFH and can never be changed	Parameter ID MSB
18h	FFh	Reserved	
...(1)	FFh	Reserved	
2Fh	FFh	Reserved	
30h	E5h	Bit[7:5]=111 Reserved Bit[4:3]=00 Non-volatile Status Register Bit[2]=1 Page Programmable Bit[1:0]=01 Supports 4KB Erase	
31h	20h	4K-Byte Erase Opcode	
32h	F9h	Bit[7] =1 Reserved Bit[6] =1 Supports (1-1-4) Fast Read Bit[5] =1 Supports (1-4-4) Fast Read Bit[4] =1 Supports (1-2-2) Fast Read Bit[3] =1 Support Dual Transfer Rate Bit[2:1]=00 3-Byte/24-Bit Only Addressing Bit[0] =1 Supports (1-1-2) Fast Read	
33h	FFh	Reserved	
34h	FFh	Flash Size in Bits	128 Mega Bits = 07FFFFFFh
35h	FFh	Flash Size in Bits	
36h	FFh	Flash Size in Bits	
37h	07h	Flash Size in Bits	
38h	44h	Bit[7:5]=010 8 Mode Bits are needed Bit[4:0]=00100 16 Dummy Bits are needed	Fast Read Quad I/O Setting
39h	EBh	Quad Input Quad Output Fast Read Opcode	
3Ah	08h	Bit[7:5]=000 No Mode Bits are needed Bit[4:0]=01000 8 Dummy Bits are needed	Fast Read Quad Output Setting
3Bh	6Bh	Single Input Quad Output Fast Read Opcode	
3Ch	08h	Bit[7:5]=000 No Mode Bits are needed Bit[4:0]=01000 8 Dummy Bits are needed	Fast Read Dual Output Setting
3Dh	3Bh	Single Input Dual Output Fast Read Opcode	
3Eh	80h	Bit[7:5]=100 8 Mode bits are needed Bit[4:0]=00000 No Dummy bits are needed	Fast Read Dual I/O Setting
3Fh	BBh	Dual Input Dual Output Fast Read Opcode	
40h	FEh	Bit[7:5]=111 Reserved Bit[4]=1 support (4-4-4) Fast Read Bit[3:1]=111 Reserved Bit[0]=0 Not support (2-2-2) Fast Read	
41h	FFh	Reserved	
42h	FFh	Reserved	
43h	FFh	Reserved	

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
44h	FFh	Reserved	
45h	FFh	Reserved	
46h	00h	No Mode Bits or Dummy Bits for (2-2-2) Fast Read	
47h	00h	Not support (2-2-2) Fast Read	
48h	FFh	Reserved	
49h	FFh	Reserved	
4Ah	44h	Bit[7:5]=010 Mode bits are needed Bit[4:0]=00100 16 Dummy bits are needed	
4Bh	EBh	QPI Fast Read Opcode	
4Ch	0Ch	Sector Type 1 Size (4KB)	Sector Erase Type & Opcode
4Dh	20h	Sector Type 1 Opcode	
4Eh	0Fh	Sector Type 2 Size (32KB)	
4Fh	52h	Sector Type 2 Opcode	
50h	10h	Sector Type 3 Size (64KB)	Sector Erase Type & Opcode
51h	D8h	Sector Type 3 Opcode	
52h	00h	Sector Type 4 Size (256KB) – Not supported	
53h	00h	Sector Type 4 Opcode – Not supported	
54h	34h	Bit[31:25]=1111,111 Erase type4 not exist Bit[24:18]=0,1011,11 Erase type3 erase typical time= 250ms/256ms Bit[17:11]=01,0110,0 Erase type2 erase typical time= 200ms/208ms Bit[10:4]=010,0011, Erase type1 erase typical time= 50ms/64ms Bit[3:0]=0100Multiplier from typical erase time to maximum erase time	Typical Erase Times and Multiplier Used to Derive Max Erase Times
55h	62h		
56h	BDh		
57h	FEh		
58h	82h	Bit[7:4]=1000 Page size= 256 Bytes Bit[3:0]=0010 Multiplier from typical time to maximum time for Page or Byte program	Chip Erase Typical Time, Byte Program and Page Program Typical Times, Page Size
59h	E7h	Bit[31]=0 Reserved Bit[30:24]=100,1100,Chip erase typical time= 50s/52s Bit[23:19]=0000,0 Reserved Bit[18:14]=100,11 First Byte program=30us/32us Bit[13:8]=10,0111 Page program time= 500us/512us	
5Ah	04h		
5Bh	4Ch		
5Ch	88h	Bit[7:4]=1000 Prohibited Operations During Erase Suspend Bit[3:0]=1000 Prohibited Operations During Program Suspend	Erase/Program Suspend/Resume Support, Intervals, Latency, Keep Out Areas Size
5Dh	15h	Bit[12:9]=0001 Program Resume to Suspend Interval Time = 100us/ 128us Bit[8]=0 Reserved	
5Eh	17h	Bit[23:20]=0001 Erase Resume to Suspend Interval Time = 100us/ 128us Bit[19:13]=0111,101 Suspend in-progress Program Max Latency Time= 30us/30us	
5Fh	3Dh	Bit[31]=0 Suspend/Resume Supported Bit[30:24]=011,1101 Suspend in-progress Erase Max Latency Time= 30us/30us	

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
60h	7Ah	Program Resume Instruction	Program/Erase Suspend/Resume Instructions
61h	75h	Program Suspend Instruction	
62h	7Ah	Resume Instruction	
63h	75h	Suspend Instruction	
64h	04h	Bit[31]=0 Support deep power down	Deep Power down and Status Register Polling Device Busy
65h	B3h		
66h	D5h	Bit[30:23]=B9h=101,1100,1 Enter Deep Power down Instruction	
67h	5Ch	Bit[22:15]=ABh=101,0101,1 Exit Deep Power down Instruction Bit[14:8]=011,0011, Exit Deep Power down to next operation delay =20us/20us Bit[7:2]=0000,01 Use of legacy polling is supported by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy) Bit[1:0]=00 Reserved	
68h	11h	Bit[3:0]=0001 4-4-4 mode disable: issue FFh instruction Bit[8:4]=0,0001 enter 4-4-4 mode: set QE then issue instruction 38h	Hold and WP Disable Function, Quad Enable Requirements, 4-4-4 Mode Enable/Disable Sequences, 0-4-4 Entry/Exit Methods and Support
69h	06h	Bit[9]=1 Support 0-4-4 Bit[15:10]=0000,01 M<7:0>=00H, 0-4-4 Mode Exit Method	
6Ah	C4h	Bit[19:16]=0100 M<7:0>=AXH, 0-4-4 Mode Entry Method Bit[22:20]=100 QE is in status register 2, bit 1 Bit[23]=1 support HOLD or RESET Disable	
6Bh	00h	Reserved	
6Ch	08h	Bit[6:0]=0001000 Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1 Bit[7]=0 Reserved	32-bit Address Entry/Exit Methods and Support, Soft Reset and Rescue Sequences, Volatile and Nonvolatile Status Register Support
6Dh	10h	Bit[13:8]=010000 Soft Reset and Rescue Sequence Support(66H-99H)	
6Eh	80h	Bit[23:14]=1000000000 Reserved	
6Fh	80h	Bit[31:24]=10000000 Reserved	
70h	FFh	Reserved	
…	…	…	
8Fh	FFh	Reserved	
90h	00h	Bit[15:0]=h2000 Maximum Supply Voltage is 2.0V	Vcc Supply Voltage
91h	20h		
92h	50h	Bit[31:16]=h1650 Minimum Supply Voltage is 1.65V	
93h	16h		
94h	9E	Bit[0]=0 not support Hardware Reset# pin Bit[1]=1 Support Hardware Hold# pin Bit[2]=1 Support Deep Power Down Mode Bit[3]=1 Support Software Reset Bit[11:4]=10011001 Software Reset Opcode Bit[12]=1 Support Program Suspend/Resume Bit[13]=1 Support Erase Suspend/Resume	

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
		Bit[14]=1 Reserved Bit[15]=1 Support Wrap-Around Read mode	
95h	F9		
96h	77h	Wrap-Around Read mode Opcode	
97h	64h	64H: support 8B&16B&32B&64B wrap-around read	
98h	D9h	Bit[0]=1 support Individual block lock Bit[1]=0 Volatile Individual block lock blt Bit[9:2]=00,1101,10 Individual block lock Opcode Bit[10]=0 default protect Bit[11]=1 support Secured OTP Bit[12]=0 not support Read Lock Bit[13]=0 not support Permanent Lock Bit[15:14]=11 Reserved	
99h	C8h		
9Ah	FFh	Reserved	
9Bh	FFh	Reserved	
...[1]	FFh	Reserved	
FFh	FFh	Reserved	

Notes:
1. Data stored in Byte Address9Ch toFFh arereserved, thevalue isFFh.
2. 1Dword=4 Bytes
3. PID(x)= Parameter IdentificationTable (x)

10.2.30. Erase Security Sector(44h)

The FM25LQ128I3 offers one 4x256-byte Security Sector. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Sector instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Sector Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code "44h" followed by a 24-bit address A23-A0 to erase the Security Sector.

A23-16	A15-12	A11-8	A7-0
00h	0 0 0 0	0 0 0 0	Don't Care

The Erase Security Sector instruction sequence is shown in Figure 60. The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After CS# is driven high, the self-timed Erase Security Sector operation will commence for a time duration of t_{SE} (See "11.6AC Electrical Characteristics"). While the Erase Security Sector cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Sector cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Sector Lock Bit (LB) in the Status Register-2 can be used to OTP protect the Security Sector. Once a lock bit is set to 1, the Security Sector will be permanently locked and Erase Security Sector instruction will be ignored.
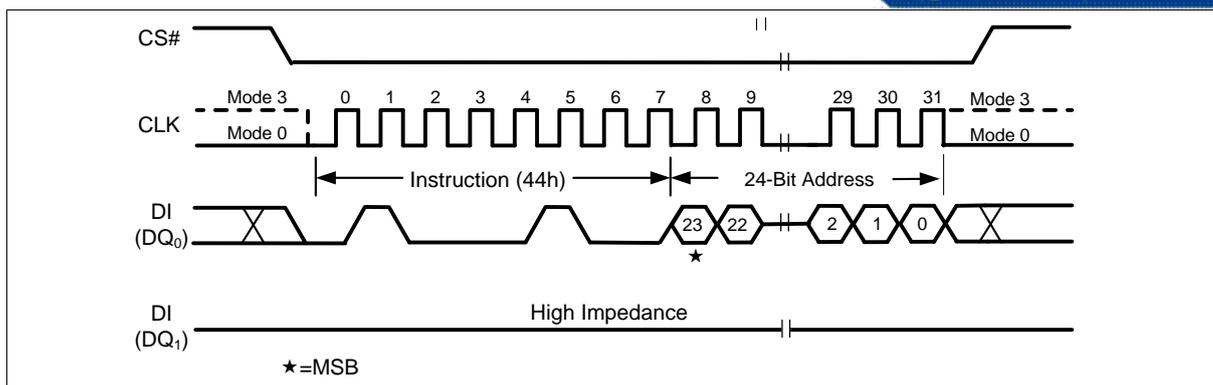
Figure 60Erase Security Sector Instruction (SPI Mode only)

10.2.31. Program Security Sector (42h)

The Program Security Sector instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of Security Sector data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Sector Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code "42h" followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Sector page0	00h	0 0 0 0	0 0 0 0	Don't Care
Security Sector page1	00h	0 0 0 0	0 0 0 1	Don't Care
Security Sector page2	00h	0 0 0 0	0 0 1 0	Don't Care
Security Sector page3	00h	0 0 0 0	0 0 1 1	Don't Care

The Program Security Sector instruction sequence is shown inFigure 61. The Security Sector Lock Bit (LB) in the Status Register-2 can be used to OTP protect the Security Sector. Once a lock bit is set to 1, the Security Sector will be permanently locked and Program Security Sector instruction will be ignored.
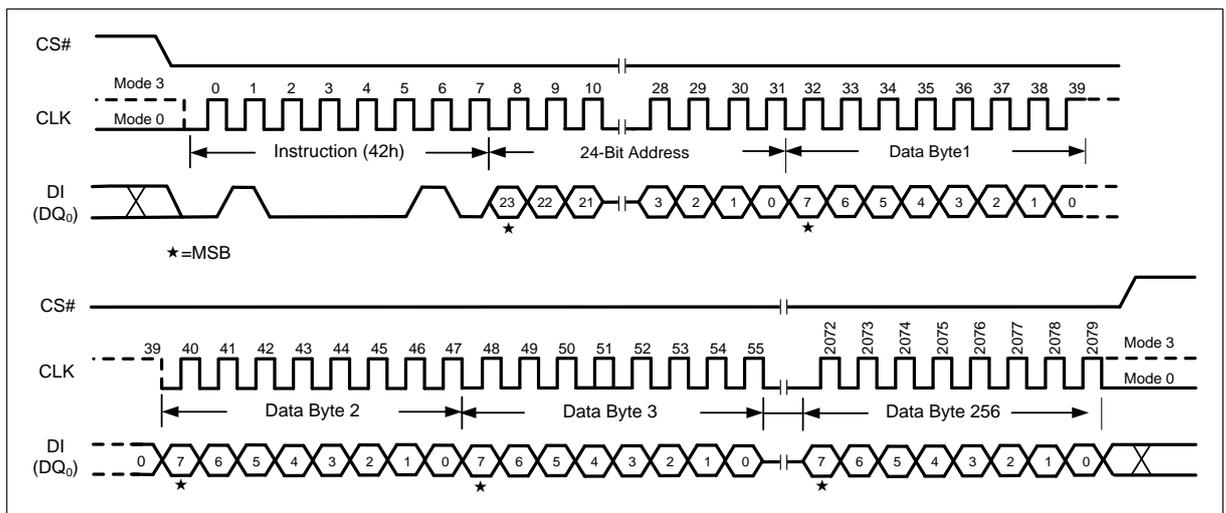

Figure 61 Program Security Sector Instruction (SPI Mode only)

10.2.32. Read Security Sector (48h)

The Read Security Sector instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from the Security Sector. The instruction is initiated by driving the CS# pin low and then shifting the instruction code "48h" followed by a 24-bit address A23-A0 and eight "dummy" clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin.

After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte FFh), it will be reset to 00h, the first byte of the register, and continues to increment. The instruction is completed by driving CS# high. The Read Security Sector instruction sequence is shown in Figure 62.

If a Read Security Sector instruction is issued while an Erase, Program or Write cycle is in process (WIP =1), the instruction is ignored and will not have any effect on the current cycle. The Read Security Sector instruction allows clock rates from D.C. to a maximum of FR (see "11.6AC Electrical Characteristics").

| ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Sector page0	00h	0 0 0 0	0 0 0 0	Don't Care
Security Sector page1	00h	0 0 0 0	0 0 0 1	Don't Care
Security Sector page2	00h	0 0 0 0	0 0 1 0	Don't Care
Security Sector page3	00h	0 0 0 0	0 0 1 1	Don't Care
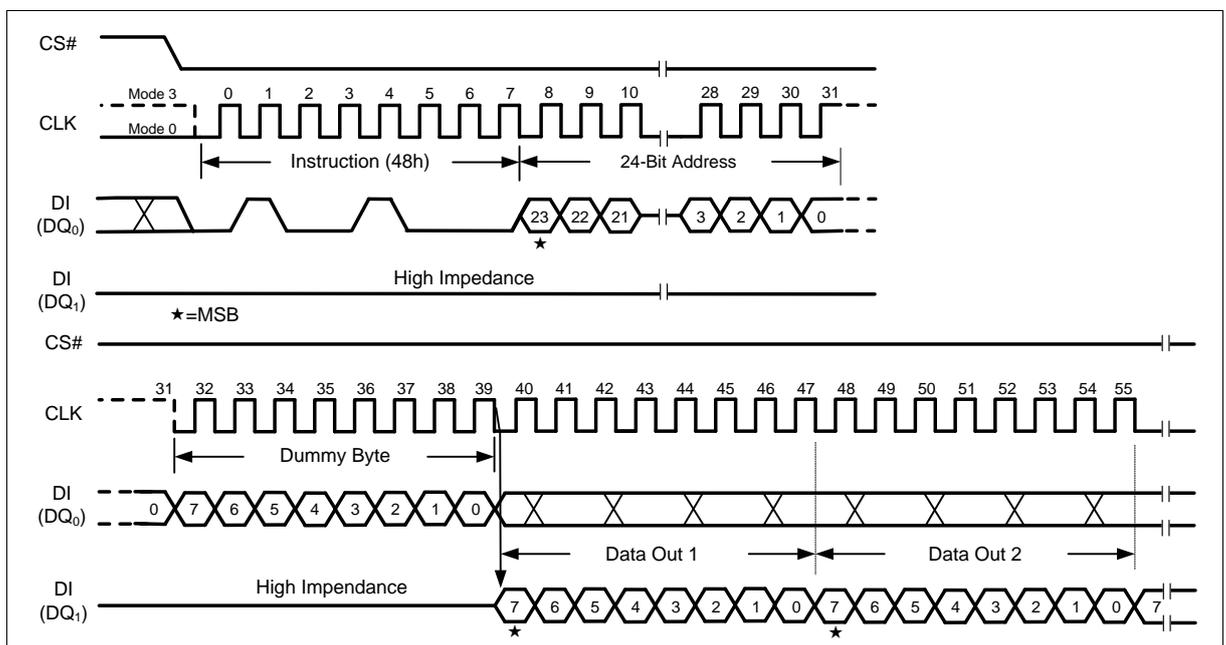
Figure 62 Read Security Sector Instruction (SPI Mode only)

10.2.33. Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, "Set Read Parameters (C0h)" instruction can be used to configure the number of dummy clocks for "Fast Read (0Bh)", "Fast Read Quad I/O (EBh)" , "DTR Fast Read Quad I/O (EDh)"& "Burst Read with Wrap (0Ch)" instructions, and to configure the number of bytes of "Wrap Length" for the "Burst Read with Wrap (0Ch)" instruction.

In Standard SPI mode, the "Set Read Parameters (C0h)" instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer toTable8~Table 10 the Instruction set for details. The "Wrap Length" is set by W5-4 bit in the "Set Burst with Wrap (77h)" instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default "Wrap Length" after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 4.

| P5 – P4	STR FAST READ		DTR FAST READ		P1 – P0	WRAP LENGTH
	DUMMY CLOCKS	MAXIMUM READ FREQ.	DUMMY CLOCKS	MAXIMUM READ FREQ.		
0 0	4	80MHz	10	104MHz	0 0	8-byte
0 1	6	108MHz	8	80MHz	0 1	16-byte
1 0	8	133MHz	10	104MHz	1 0	32-byte
1 1	10	133MHz	10	104MHz	1 1	64-byte
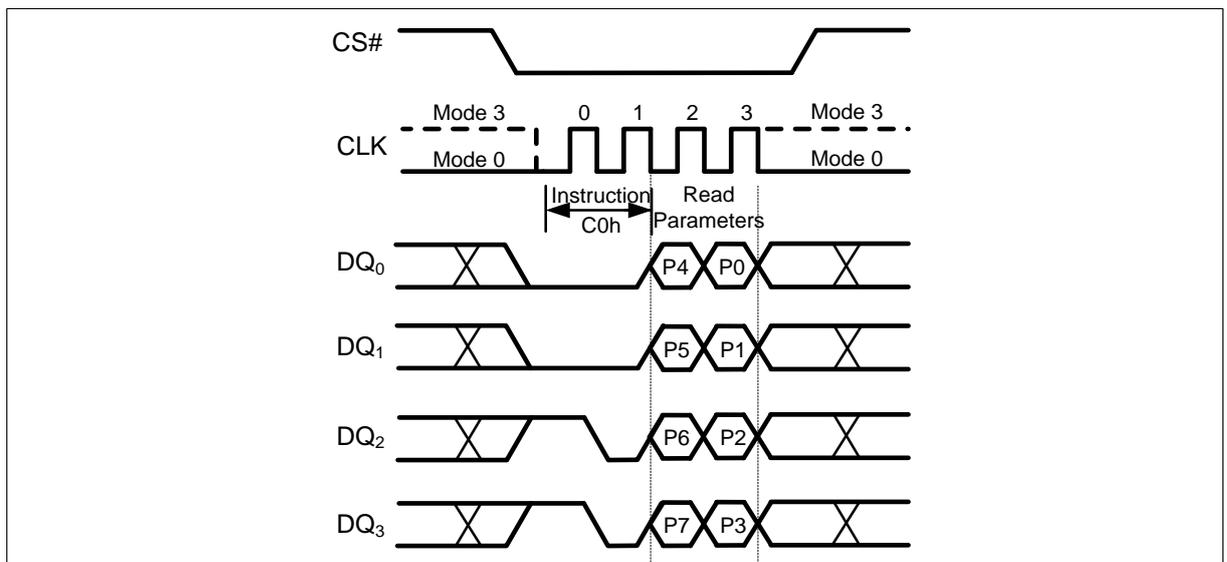
Figure 63 Set Read Parameters Instruction (QPI Mode only)

10.2.34. Burst Read with Wrap (0Ch)

The "Burst Read with Wrap (0Ch)" instruction provides an alternative way to perform the read operation with "Wrap Around" in QPI mode. The instruction is similar to the "Fast Read (0Bh)" instruction in QPI mode, except the addressing of the read operation will "Wrap Around" to the beginning boundary of the "Wrap Length" once the ending boundary is reached.

The "Wrap Length" and the number of dummy clocks can be configured by the "Set Read Parameters C0h)" instruction.
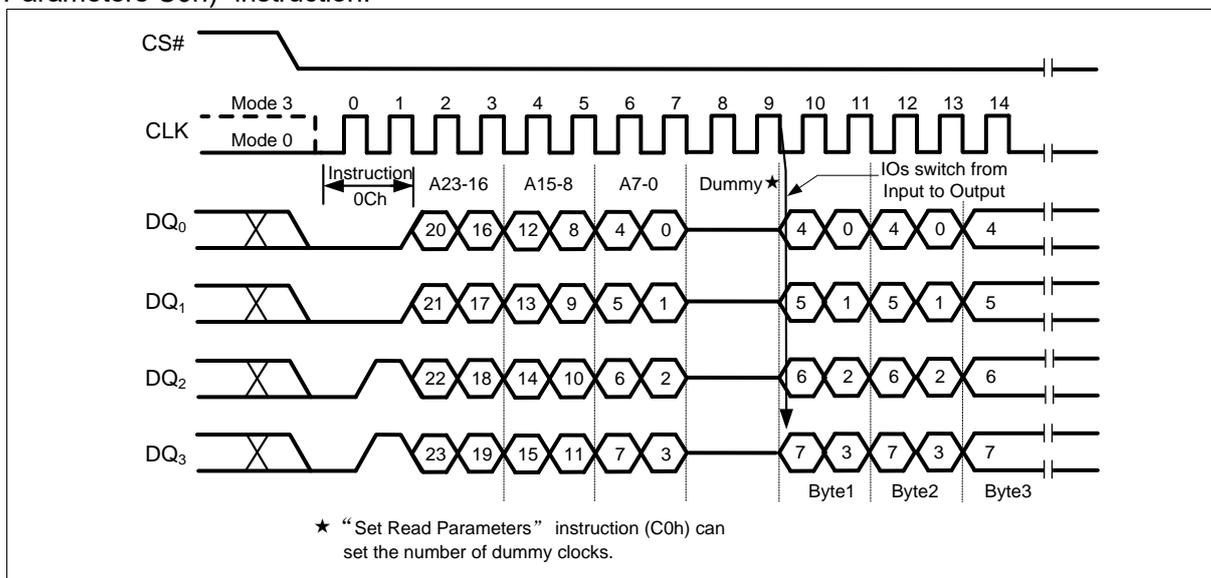
Figure 64 Burst Read with Wrap Instruction (QPI Mode only)

10.2.35. Enable QPI (38h)

TheFM25LQ128I3supportbothStandard/Dual/QuadSerialPeripheralInterface(SPI)andQuad Peripheral Interface (QPI). However, SPI mode and QPI mode can not be used at the same time. "Enable QPI (38h)" instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set to 1 first, and an "Enable QPI (38h)" instruction must be issued. If the Quad Enable (QE) bit is 0, the "Enable QPI (38h)" instruction will be ignored and the device will remain in SPI mode.

See "Table 10" for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/EraseSuspend status, and the Wrap Length setting will remain unchanged.
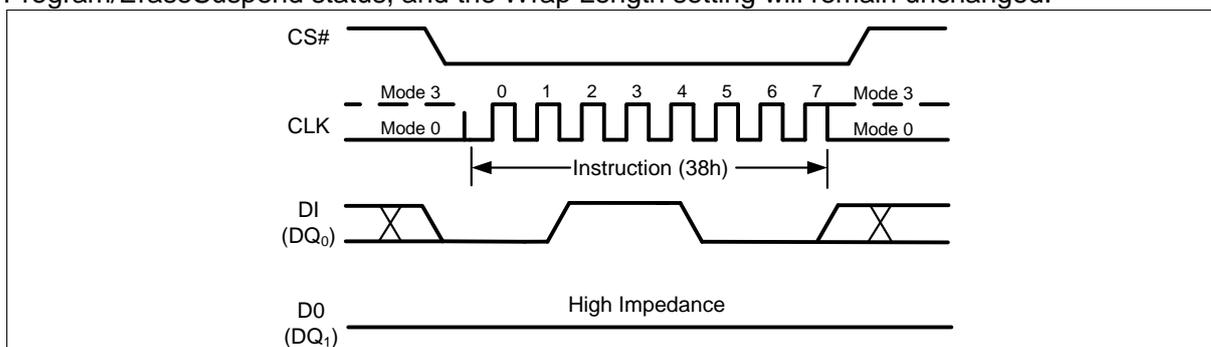

Figure 65 Enable QPI Instruction (SPI Mode only)

10.2.36. Disable QPI (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, a "Disable QPI (FFh)" instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) andProgram/Erase Suspend status and the Wrap Length setting will remain unchanged.
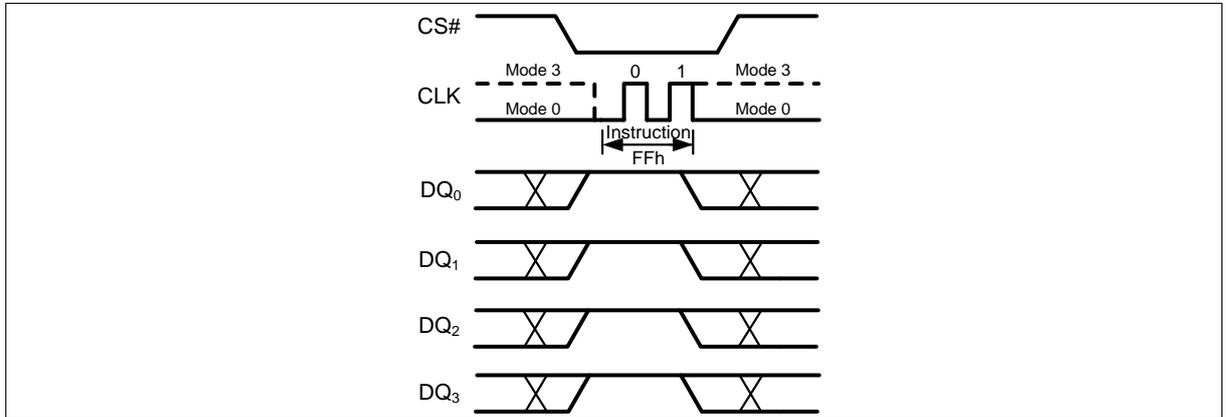

Figure 66 Disable QPI Instruction (QPI Mode only)

10.2.37. Individual Block/Sector Lock(36h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-2 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC,TB, BP2, BP1 and BP0 bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default value after power up or after Reset is 1, so the entire memory array is being protected.

To lock a specific block or sector as illustrated inFigure 11, an Individual Block/Sector Lock command must be issued by driving CS# low, shifting the instruction code "36h" into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high.

A Write Enable instruction must be executed before the device will accept the Individual Block/Sector Lock Instruction (Status Register bit WEL= 1).
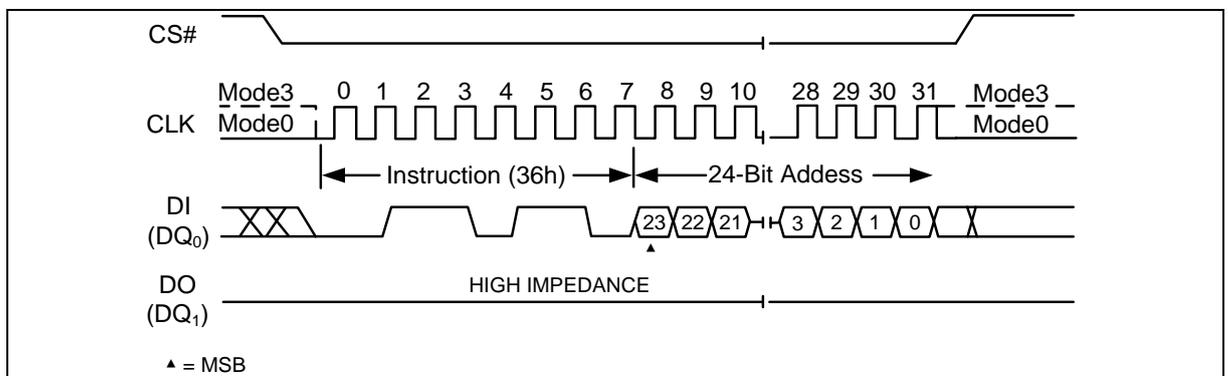

**Figure 67 Individual Block/Sector Lock Instruction(SPI)**
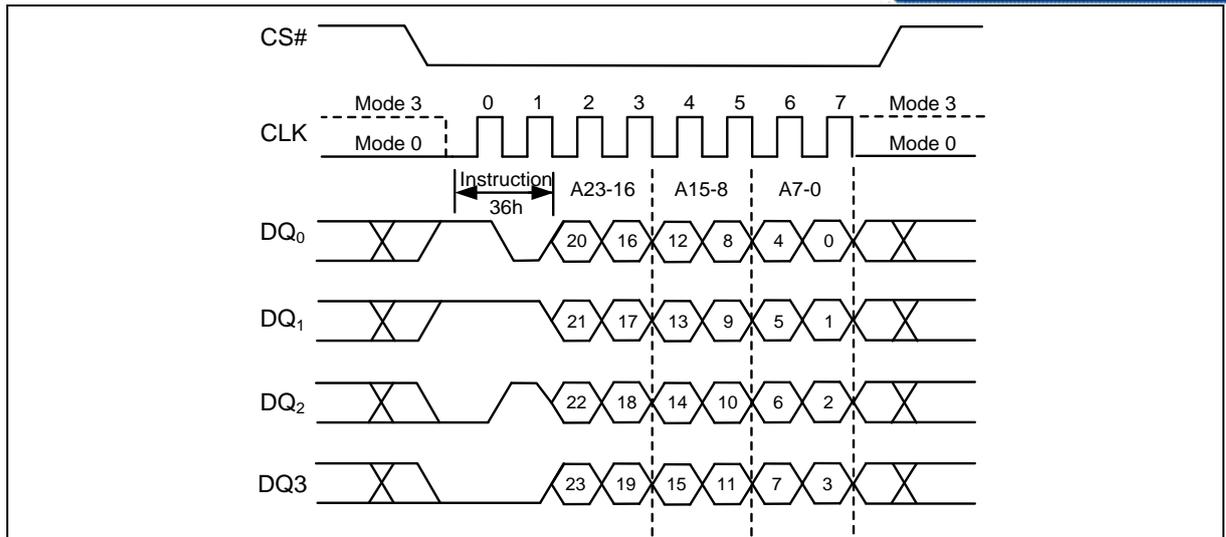
Figure 68 Individual Block/Sector Lock Instruction(QPI Mode)

10.2.38. Individual Block/Sector Unlock(39h)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-2 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC,TB, BP2, BP1 and BP0 bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default value after power up or after Reset is 1, so the entire memory array is being protected.

To unlock a specific block or sector as illustrated inFigure 11, an Individual Block/Sector Lock command must be issued by driving CS# low, shifting the instruction code "39h" into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high.

A Write Enable instruction must be executed before the device will accept the Individual Block/Sector Unlock Instruction (Status Register bit WEL= 1).
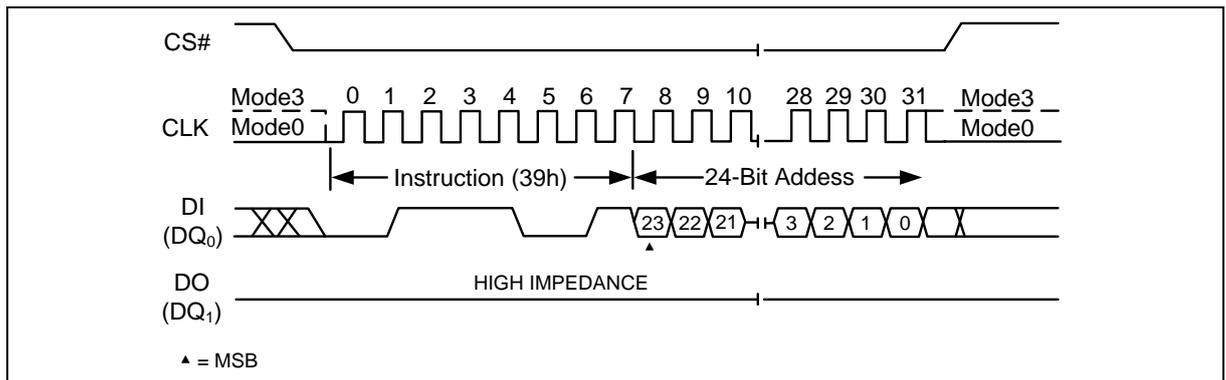

**Figure 69 Individual Block/Sector Unlock Instruction (SPI Mode)**
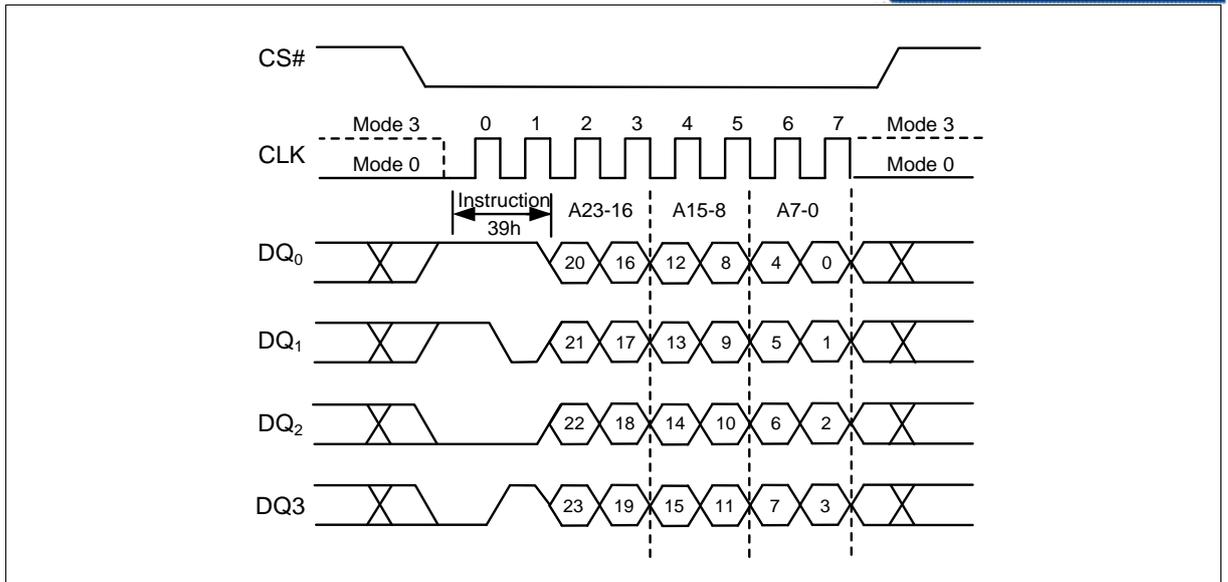
Figure 70 Individual Block/Sector Unlock Instruction (QPI Mode)

10.2.39. Read Block/Sector Lock (3Dh)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-2 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC,TB, BP2,BP1 and BP0 bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default value after power up or after Reset is 1, so the entire memory array is being protected.

To read out the lock bit of a specific block or sector as illustrated inFigure 11,a Read Block/Sector Lock command must be issued by driving CS# low, shifting the instruction code "3Dh" into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high. The Block/Sector Lock bit value will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) as shown in. If the least significant bit (LSB) is 1, the corresponding block/sector is locked; if LSB=0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.
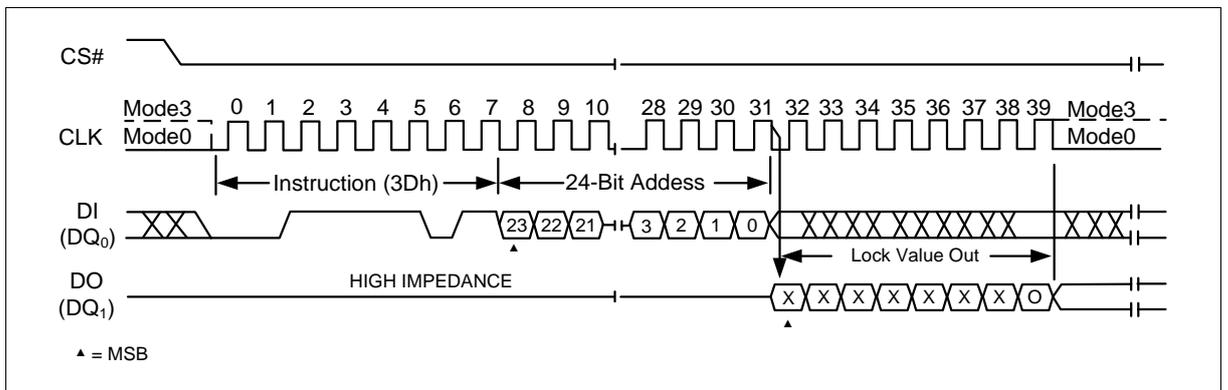

**Figure 71 Read Block/Sector Lock Instruction (SPI Mode)**
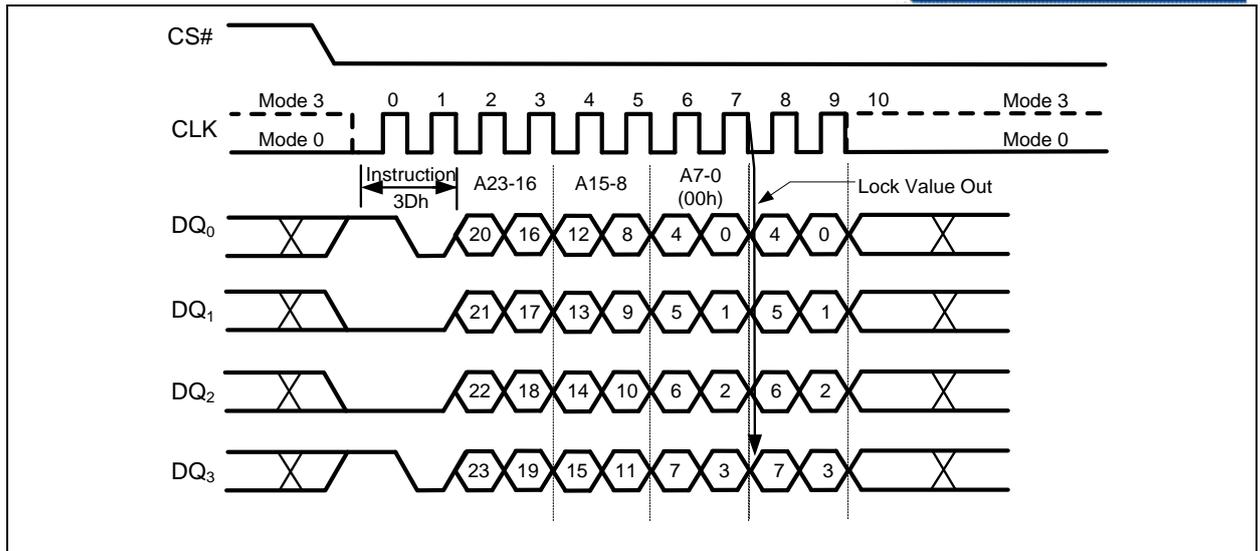
Figure 72 Read Block/Sector Lock Instruction (QPI Mode)

10.2.40. Global Block/Sector Lock (7Eh)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock instruction. The command must be issued by driving CS# low, shifting the instruction code "7Eh" into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

A Write Enable instruction must be executed before the device will accept the Global Block/Sector Lock Instruction (Status Register bit WEL= 1).
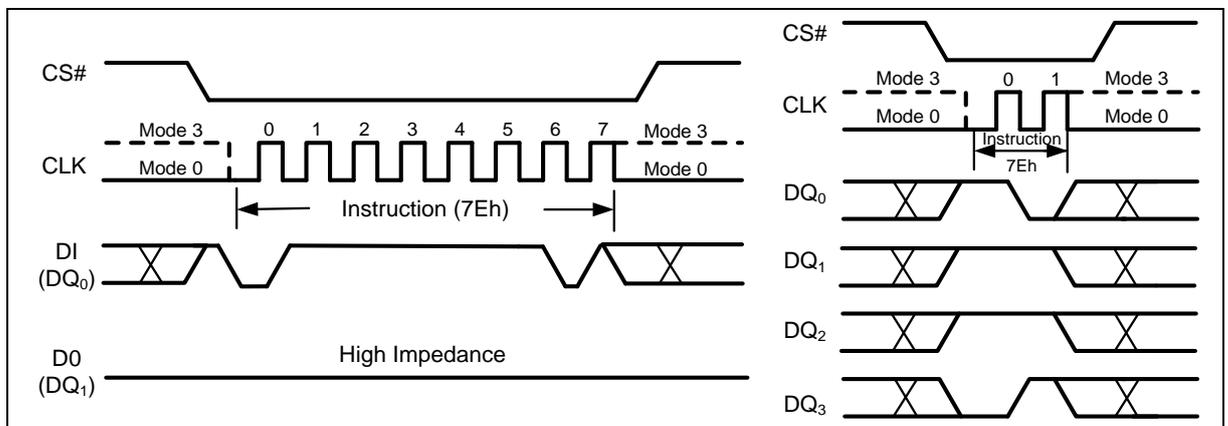
Figure 73 Global Block/Sector Lock Instruction for SPI Mode (left) or QPI Mode (right)

10.2.41. Global Block/Sector Unlock (98h)

All Block/Sector Lock bits can be set to 0 by the Global Block/Sector Unlock instruction. The command must be issued by driving CS# low, shifting the instruction code "98h" into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

A Write Enable instruction must be executed before the device will accept the GlobalBlock/Sector Unlock Instruction (Status Register bit WEL= 1).
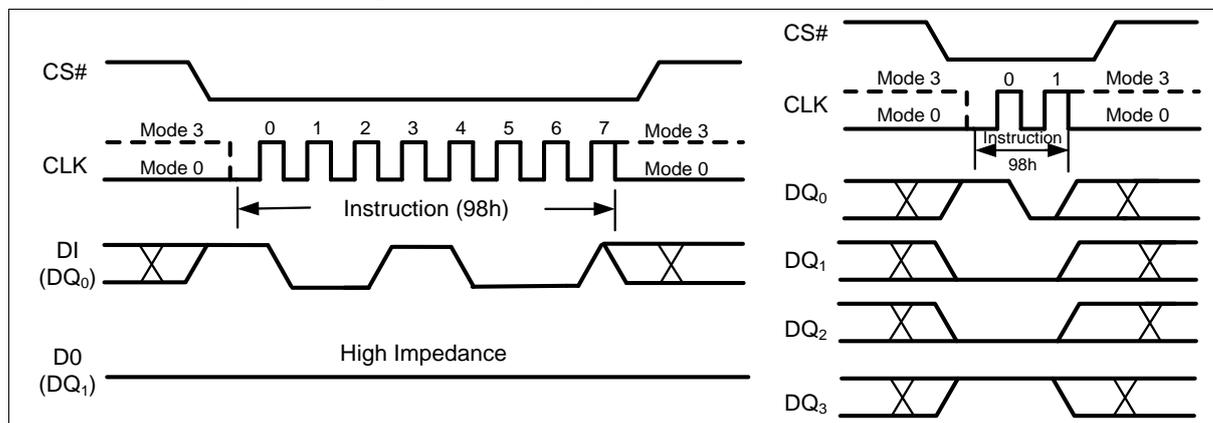

Figure 74　Global Block/Sector Unlock Instruction for SPI Mode (left) or QPI Mode (right)

10.2.42. Enable Reset (66h) and Reset (99h)

FM25LQ128I3 provide a software Reset instruction. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Read parameter setting P7-P0, Continuous Read Mode bit setting M7-M0 and Wrap Bit setting W6-W4.

"Enable Reset (66h)" and "Reset (99h)" instructions can be issued in either SPI mode or QPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately 100μs to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit in Status Register before issuing the Reset command sequence.
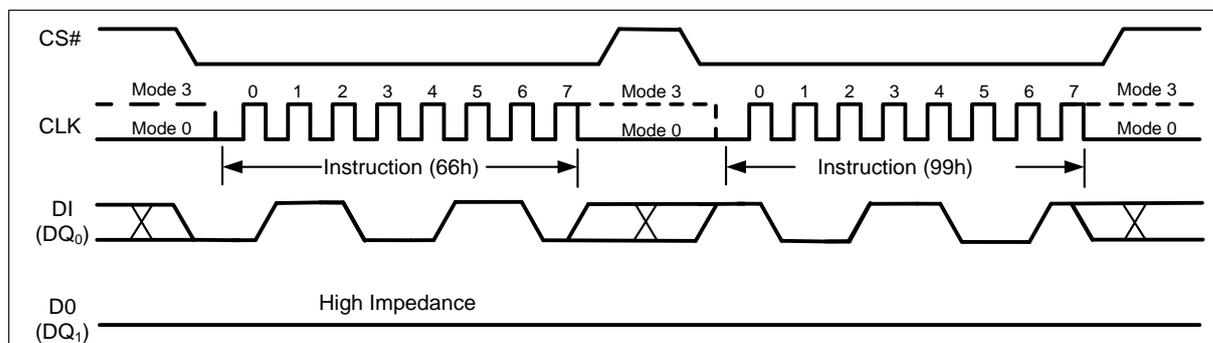

**Figure 75　Enable Reset and Reset Instruction Sequence (SPI Mode)**
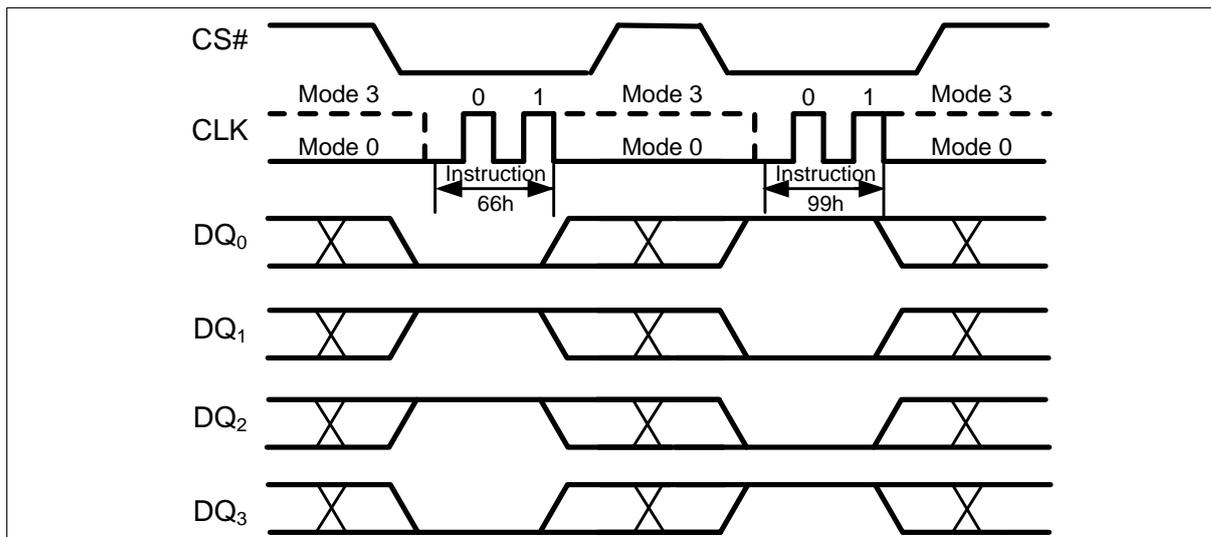
**Figure 76 Enable Reset and Reset Instruction Sequence (QPI Mode)**

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on I/O Pin with Respect to Ground	-0.6V to V_{CC}+0.5V
Transient Input/Output Voltage(note: overshoot<20ns)	-2.0V to V_{CC} +2.0V
V_{CC}	-0.6V to 2.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 77Maximum Negative Overshoot WaveformFigure 78Maximum Positive Overshoot Waveform
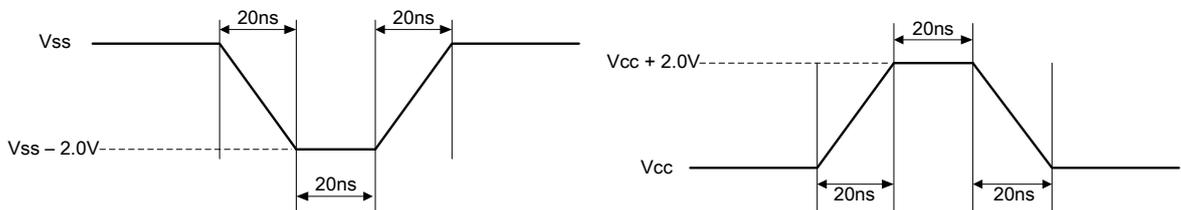
11.2. Pin Capacitance

Applicable over recommended operating range from: T_A = 25°C, f = 1MHz.

Symbol	Test Condition	Max	Units	Conditions
C_{IN}[1]	Input Capacitance	6	pF	V_{IN} = 0V
C_{OUT}[1]	Output Capacitance	8	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

11.3. Power-upTiming

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 1.65V to 2.0V, (unless otherwise noted).

Symbol	PARAMETER	SPEC MIN	SPEC MAX	UNIT
t_{VSL}	VCC (min) to CS# Low	2.5		ms
V_{WI}	Write Inhibit Threshold Voltage	1	1.4	V
V_{PWD}	VCC voltage needed to below $V_{PWD}$for ensuring initialization will occur		0.4	V
t_{PWD}	The minimum duration for ensuring initialization will occur	100		us

**Note:** 1. this parameter is characterized and is not 100% tested.
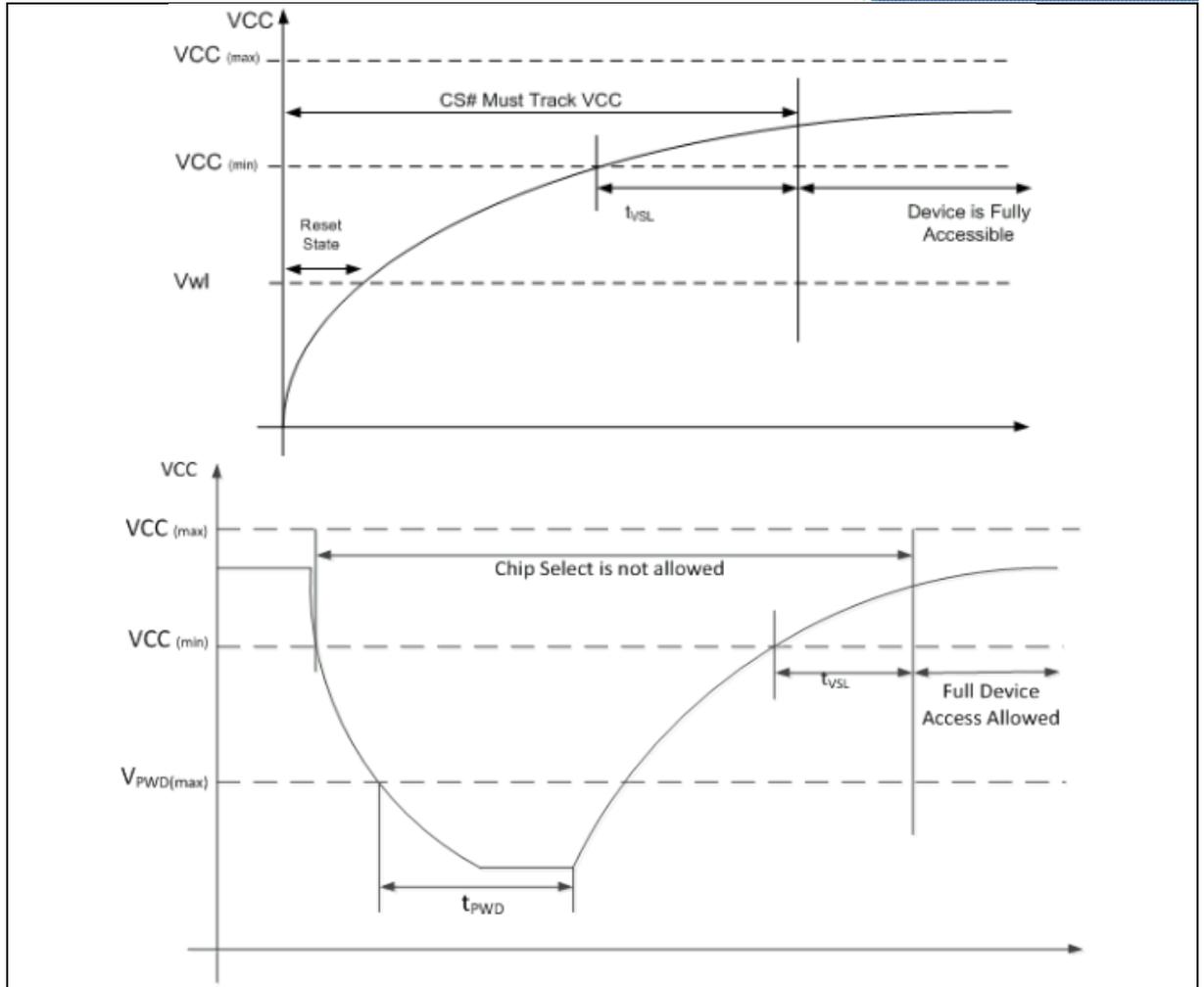
Figure 79 Power-up Timing& Power Up/Down and Voltage Drop

11.4. DC Electrical Characteristics

Table 12   DC Characteristics

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 1.65V to 2.0V, (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
V_{cc}	Supply Voltage		1.65		2.0	V
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
I_{CC1}	Standby Current	CS# = V_{CC},		10	50	µA
I_{CC2}	Deep Power-down Current	V_{IN} = Vss or V_{CC}		1	15	µA
ICC3(1)	Read Current	CLK=0.1V_{CC}/0.9V_{CC} at 80MHz, DQ open		13	18	mA
		CLK=0.1V_{CC}/0.9V_{CC}, at 133MHz, DQ open		15	25	mA
I_{CC4}	Operating Current (WRSR)	CS#=V_{CC}		12	20	mA
I_{CC5}	Operating Current (PP)			12	20	mA
I_{CC6}	Operating Current (SE)			12	20	mA
I_{CC7}	Operating Current (BE)			12	20	mA
V_{IL}(2)	Input Low Voltage		-0.5		0.2V_{CC}	V
V_{IH}(2)	Input High Voltage		0.7V_{CC}		V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC}-0.2			V

Notes:
1. Checker Board Pattern.
2. V_{IL}min and V_{IH}max are reference only and are not tested.

11.5. AC Measurement Conditions

Table 13   AC Measurement Conditions

| SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
CL	Load Capacitance		20	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.1 V_{CC} to 0.8 V_{CC}		V
IN	Input Timing Reference Voltages	0.2 V_{CC} to 0.7 V_{CC}		V
OUT	Output Timing Reference Voltages	0.5V_{CC}		V
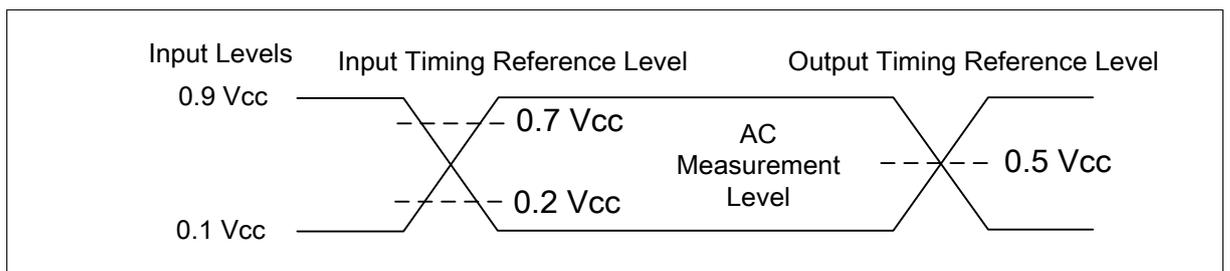
Figure 80 AC Measurement I/O Waveform

11.6. AC Electrical Characteristics

Table 14   AC Characteristics

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 1.65V to 2.0V, (unless otherwise noted).

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
F_{R1}	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR, RDSR, RDID			133	MHz
F_{R2}	Serial Clock Frequency for: Edh			104	MHz
f_R	Serial Clock Frequency for: 03h			80	MHz
t_{CH1}[1]	Serial Clock High Time	%45/ F_R			ns
t_{CL1}[1]	Serial Clock Low Time	%45/ F_R			ns
t_{CLCH}[2]	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}[2]	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time	20			ns
t_{SHQZ}[2]	Output Disable Time			7	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}	HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}	HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ}[2]	HOLD# Low to High-Z Output			12	ns
t_{HHQX}[2]	HOLD# High to Low-Z Output			7	ns
t_{CLQV}	Output Valid from CLK			7	ns
t_{WHSL}	Write Protect Setup Time before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time after CS# High	1			µs
t_{DP}[2]	CS# High to Deep Power-down Mode			20	µs
t_{RES1}[2]	CS# High to Standby Mode without Electronic Signature Read			20	µs
t_{RES2}[2]	CS# High to Standby Mode with Electronic Signature Read			20	µs
t_{SUS}[2]	CS# High to next Instruction after Suspend			40	µs
t_W	Write Status Register Cycle Time		2	25	ms
t_{BP}	Byte Program Time		30	60	us
t_{PP}	Page Program Time		0.4	2	ms
t_{SE}	Sector Erase Time		30	300	ms
t_{BE}	Block Erase Time (32KB)		150	1000	ms
t_{BE}	Block Erase Time (64KB)		200	1500	ms
t_{CE}	Chip Erase Time		40	100	s

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
t_{RST}	CS# High to Next Command After Reset(Except From Erase)			30	us
	CS# High to Next Command After Reset(From Erase)			12	ms
t_{RS}	Latency Between Resume and Next Suspend	100			μs

Notes:

1. $T_{CH1} + T_{CL1} >= 1 / F_{CLK}$;
2. This parameter is characterized and is not 100% tested.
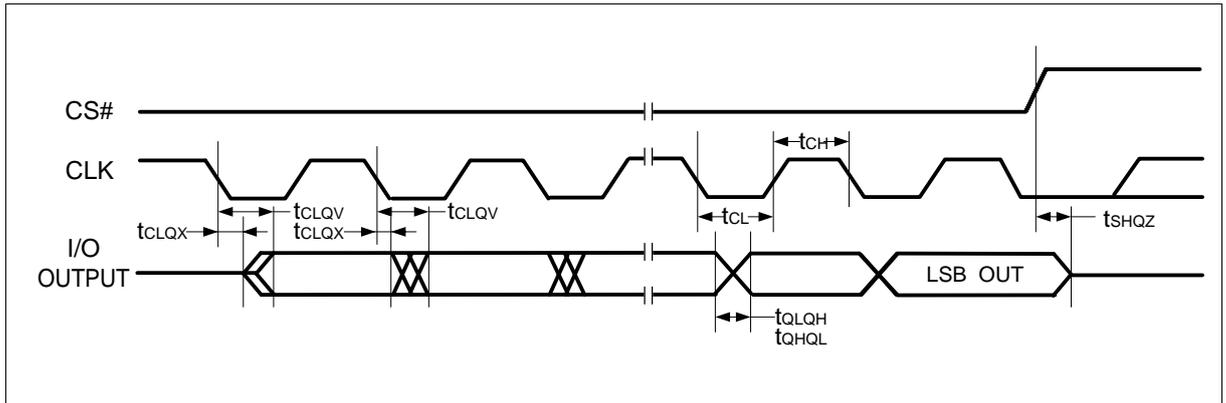
Figure 81 Serial Output Timing
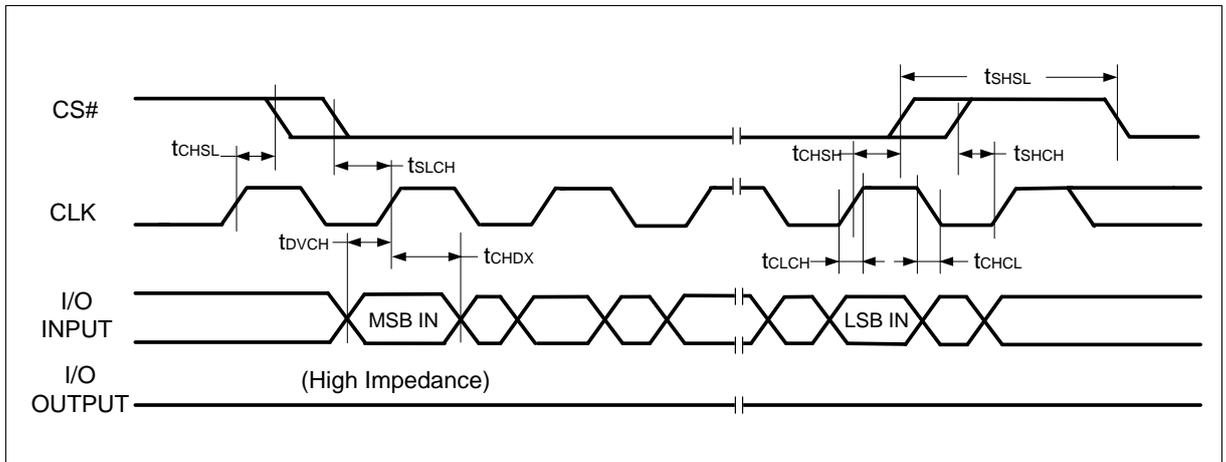

Figure 82 Serial Input Timing
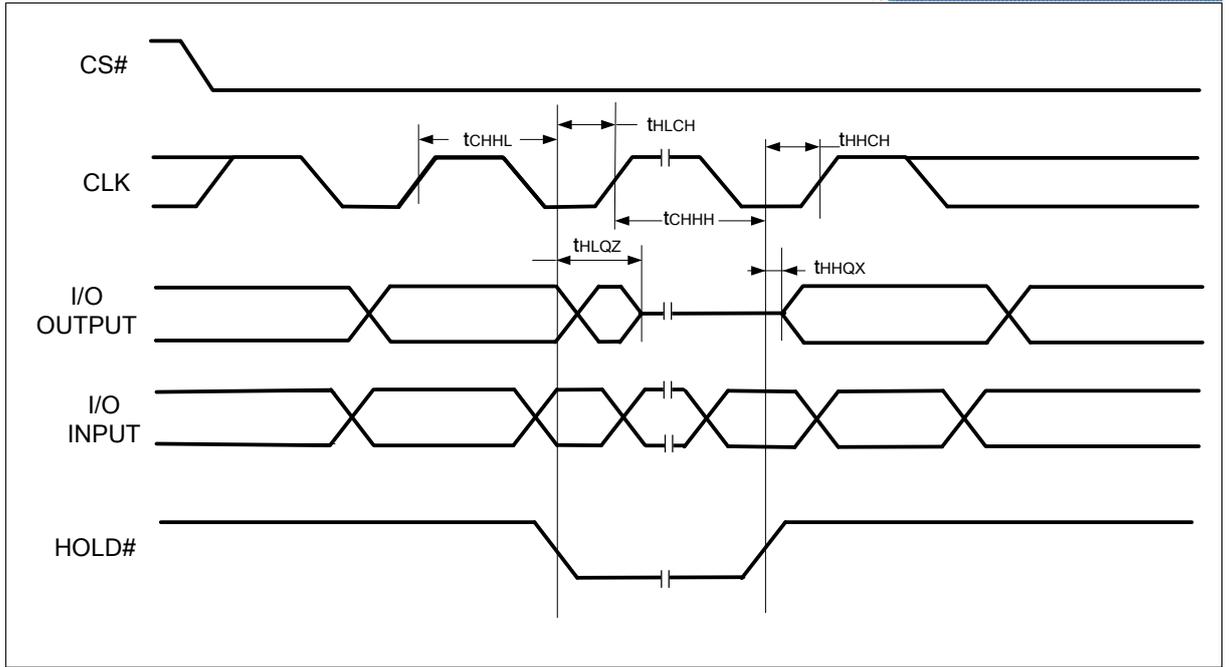
Figure 83 Hold Timing
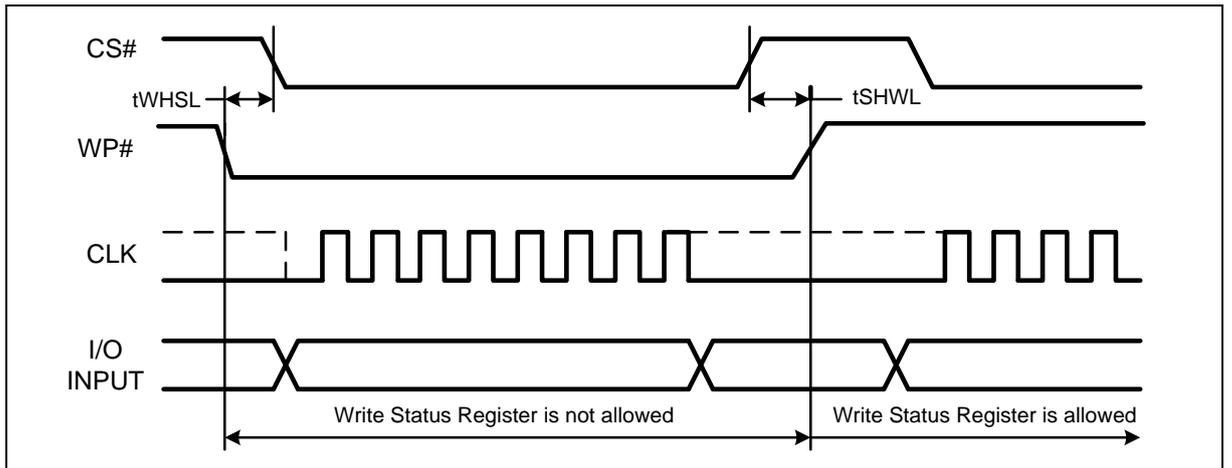
Figure 84 WP# Timing

12. Ordering Information

FM 25LQ 128I3 -XXX -C -H M -OP

Company Prefix

FM = Fudan Microelectronics Group Co.,ltd

Product Family

25LQ =1.65~2.0V Serial Flash with 4KB Uniform-Sector,
　　　Dual/Quad SPI & QPI

Product Density

128 = 128M-bit

Package Type

SOB = 8-pin SOP (208mil）
VS = 8-pin VSOP (208mil）
DNA = 8-pin TDFN (5x6mm)
BGB = 24-ball BGA (8x6mm)

Product Carrier

U = Tube
T = Tape and Reel
A = Tray

HSF ID Code

G = RoHS Compliant, Halogen-free, Antimony-free

MSL Level

3=MSL3

OPTION

Q0 = QE bit factory default value is 0
Q1 = QE bit factory default value is 1

| MPN	Package Type	Product Carrier	HSF	MSL
FM25LQ128I3-SOB-T-G3-Q0/Q1	8-pin sop (208mil)	Tape and reel	RoHS compliant, Halogen-free, Antimony-free	3
FM25LQ128I3-SOB-U-G3-Q0/Q1	8-pin sop (208mil)	Tube	RoHS compliant, Halogen-free, Antimony-free	3
FM25LQ128I3-VS-T-G3-Q0/Q1	8-pin vsop (208mil)	Tape and reel	RoHS compliant, Halogen-free, Antimony-free	3
FM25LQ128I3-VS-U-G3-Q0/Q1	8-pin vsop (208mil)	Tube	RoHS compliant, Halogen-free, Antimony-free	3
FM25LQ128I3-BGB-A-G3-Q0/Q1	24-ball BGA (8*6mm)	Tray	RoHS compliant, Halogen-free, Antimony-free	3
FM25LQ128I3-DNA-T-G3-Q0/Q1	8-pin TDFN (5*6mm)	Tape and reel	RoHS compliant, Halogen-free, Antimony-free	3
FM25LQ128I3-DNA-A-G3-Q0/Q1	8-pin TDFN (5*6mm)	Tray	RoHS compliant, Halogen-free, Antimony-free	3

13. Part Marking Scheme

13.1. SOP8 (208mil)
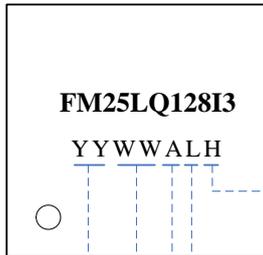
FM25LQ128I3

Y Y W W A L H

HSF ID Code

   G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the products was molded (eg..week 12)

The last two digits of the year In which the products was seal / molded.

13.2. VSOP8 (208mil)
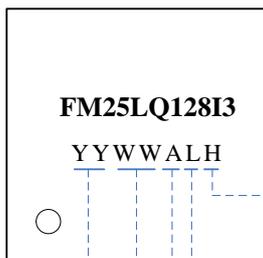
FM25LQ128I3

Y Y W W A L H

HSF ID Code

   G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

Assembly's Code

Work week during which the products was molded (eg..week 12)

The last two digits of the year In which the products was seal / molded.

13.3. TDFN8 (5x6mm)
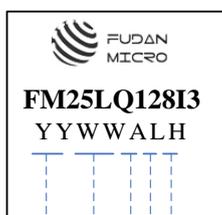
FUDAN MICRO

FM25LQ128I3

Y Y W W A L H

HSF ID Code
   G = RoHS Compliant, Halogen-free, Antimony-free
Lot Number（just with 0~9、A~Z）
Assembly's Code
Work week during which the product was molded (eg..week 12)
The last two digits of the year In which the product was sealed / molded.

13.4.   BGA24 (8x6mm)

FUDAN MICRO

FM25LQ128I3

YYWWALH

- HSF ID Code
  - **G = RoHS Compliant, Halogen-free, Antimony-free**
- **Package Lot Number (just with 0~9, A~Z)**
- **Assembly's Code**
- **Work week during which the product was molded (eg..week 12)**
- **The last two digits of the year in which the product was sealed/molded**
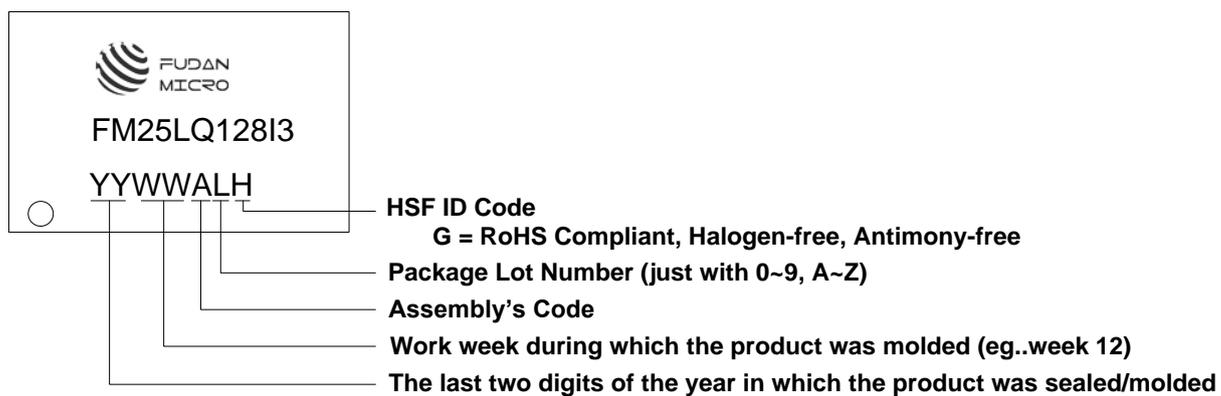
14. Packaging Information

14.1. SOP8 (208mil)

SOP 8 (208mil)

Symbol	MIN	NOM	MAX
A	– –	– –	2.150
A1	0.050	0.150	0.250
b	0.350	0.425	0.500
c	0.100	0.175	0.250
D	5.130	5.230	5.330
E1	5.180	5.280	5.380
E	7.700	7.900	8.100
e	1.270(BSC)		
L	0.500	0.675	0.850
θ	0°	4°	8°

NOTE:
1. Dimensions are in Millimeters.

14.2. VSOP8 (208mil)

VSOP8 (208mil)

Symbol	MIN	NOM	MAX
A	---	---	1.000
A1	0.050	0.100	0.150
A2	0.750	0.800	0.850
A3	0.290	0.340	0.390
b	0.380	0.420	0.460
c	0.130	0.160	0.190
D	5.180	5.280	5.380
E1	5.180	5.280	5.380
E	7.700	7.900	8.100
e	1.270(BSC)		
L	0.500	0.650	0.800
θ	0°	4°	8°

NOTE:
   1. Dimensions are in Millimeters.

14.3. TDFN8 (5x6mm)

TDFN 8 (5x6mm)
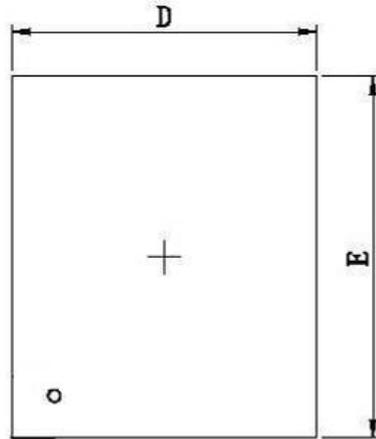
Top View
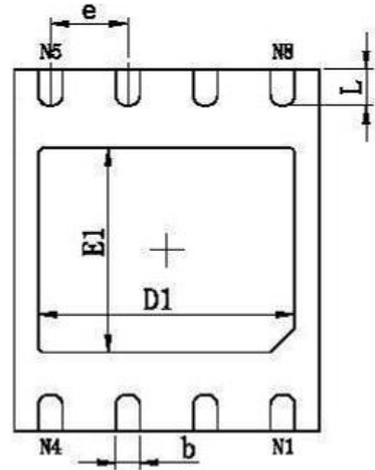
Bottom View
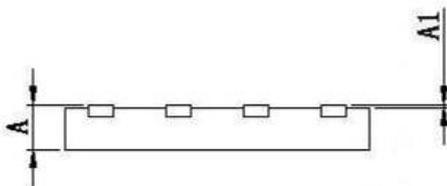
Side View

Symbol	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	0.025	0.050
D	4.900	5.000	5.100
D1	3.900	4.150	4.400
E	5.900	6.000	6.100
E1	3.300	3.400	3.500
b	0.350	0.400	0.450
e		1.270TYP	
L	0.500	0.600	0.700

NOTE:

1   Dimensions are in Millimeters.

14.4. BGA24 (8x6mm)

BGA24 (8x6mm)(5x5 Ball Array)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A(2:1)

DETAIL B(1:1)

Symbol	MIN	NOM	MAX
A	---	---	1.200
A1	0.250	0.300	0.350
A2	0.790 BSC		
D	7.900	8.000	8.100
D1	4.000 BSC		
E	5.900	6.000	6.100
E1	4.000 BSC		
e	1.000 BSC		
b	0.350	0.400	0.450

Note:
1. Dimensions are in Millimeters.
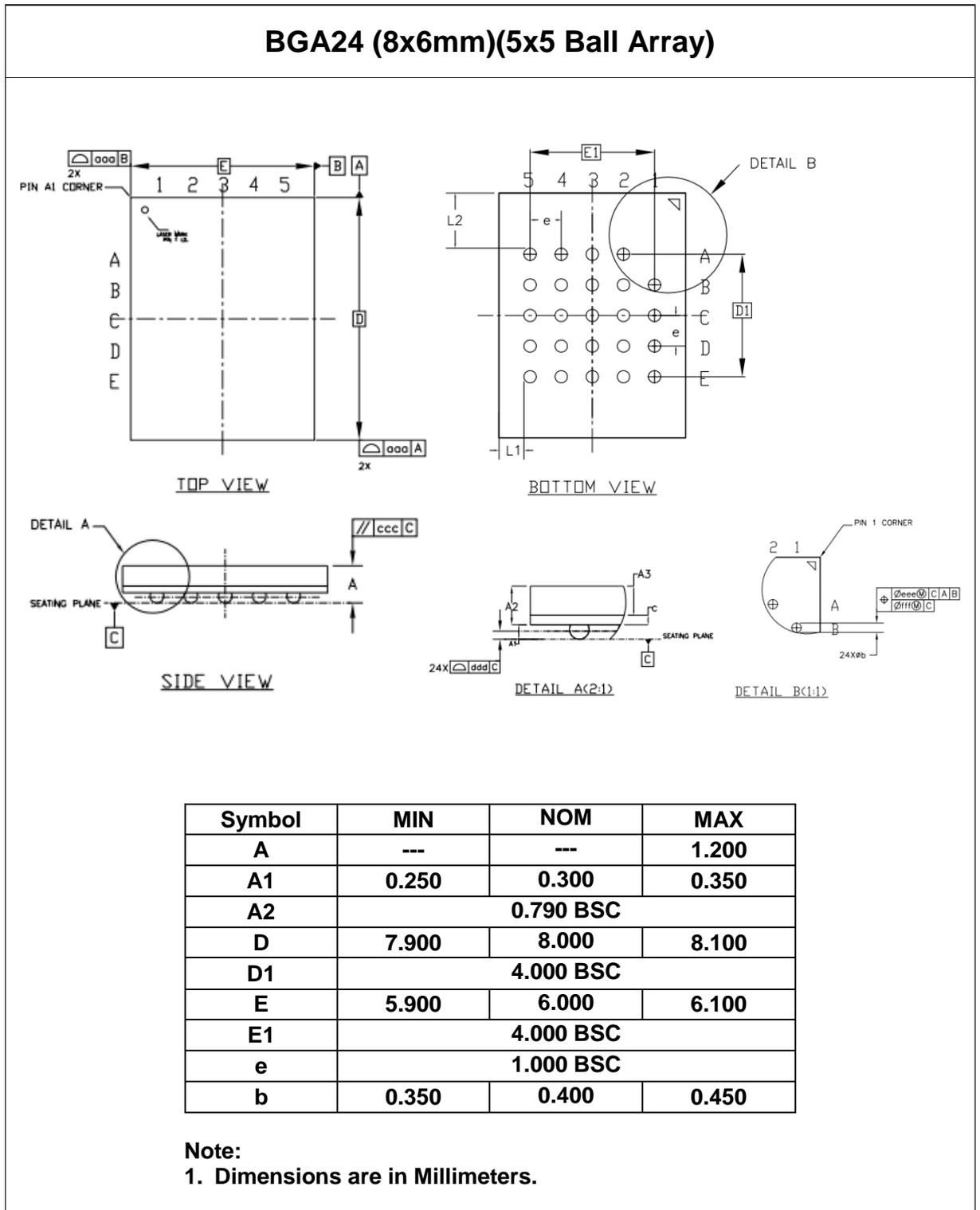
15. Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
preliminary	Nov. 2023	83		Initial Document Release.
1.0	Mar. 2024	86		1. Add VSOP8 package, 2. Update BGA24 POD, 3. Update 10.1 notes
1.1	May. 2024	85		1. Update SFDP Table 2. Update DC Electrical Characteristics 3. Update AC Electrical Characteristics 4. Update Ball Configuration BGA24
1.2	Dec. 2024	86		1. Update DC Electrical Characteristics 2. Update AC Electrical Characteristics

Sales and Service

Shanghai Fudan Microelectronics Group Co., Ltd.
Address: Bldg No. 4, 127 Guotai Rd, Shanghai City China.
Postcode: 200433
Tel: (86-021) 6565 5050 Fax: (86-021) 6565 9115

Shanghai Fudan Microelectronics (HK) Co., Ltd.
Address: Unit 506, 5/F., East Ocean Centre, 98 Granville
Road, Tsimshatsui East, Kowloon, Hong Kong
Tel: (852) 2116 3288 2116 3338
Fax: (852) 2116 0882

Beijing Office
Address: Room 423, Bldg B, Gehua Building, 1
QingLongHutong, Dongzhimen Alley north Street,
Dongcheng District, Beijing City, China.
Postcode: 100007
Tel: (86-010) 8418 6608
Fax: (86-010) 8418 6211

Shenzhen Office
Address: Room.2306-2308, Building A7, Chuangzhi
Cloud City, Liuxian Avenue, Xili Street, Nanshan District,
Shenzhen, China.
Postcode: 518000
Tel: (86-0755) 8335 0911 8335 1011 8335 2011 8335
0611
Fax: (86-0755) 8335 9011

**Shanghai Fudan Microelectronics (HK) Ltd Taiwan
Representative Office**
Address: Unit 1225, 12F., No 252, Sec.1 Neihu Rd.,
Neihu Dist., Taipei City 114, Taiwan
Tel : (886-2) 7721 1889
Fax: (886-2) 7722 3888

**Shanghai Fudan Microelectronics (HK) Ltd Singapore
Representative Office**
Address : 47 Kallang Pudding Road, #08-06,The
Crescent @ Kallang ,Singapore 349318
Tel : (65) 6443 0860
Fax: (65) 6443 1215

Fudan Microelectronics（USA）Inc.
Address : 97 E Brokaw Road, Suite 320,San Jose,CA
95112
Tel : (+1)408-335-6936

Web Site: http://www.fmsh.com/