Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM24N64

Wide Voltage Range 2-Wire Serial EEPROM

Data Sheet

Oct. 2024

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Description

The FM24N64 provides 65,536 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 8,192 words of 8 bits each, with 128-bit UID and 32-byte Security Sector. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where ultra-low power and ultra-low voltage operations are essential.

Features

- **Low Operation Voltage: V_{CC} = 1.7V to 5.5V**
- **Internally Organized: 8,192 x 8**
- **2-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bi-directional Data Transfer Protocol**
- **400Khz and 1MHz Clock Compatibility**
- **Support Software Data Protection (SWP)**
- **Support Configurable Device Address (CDA)**
- **32-Byte Page Write Modes (Partial Page Writes are Allowed)**
- **Lockable 32-Byte Security Sector**
- **128-Bit Unique ID for each device**
- **Operating Temperature**
  - **-40°C to +85°C**
- **Self-timed Write Cycle (5 ms max)**
- **High-reliability**
  - **Endurance: 4,000,000 Write Cycles**
  - **Data Retention: 100 Years**
- **SOP8, TSSOP8, USON8 and Thin 4-ball WLCSP Packages (RoHS Compliant and Halogen-free)**

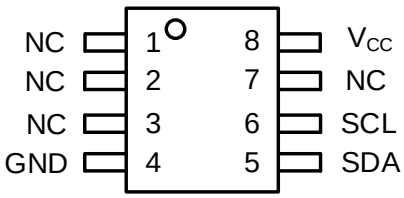
Absolute Maximum Ratings

Ambient Operating Temperature	-55℃ to +125℃
Storage Temperature	-65℃ to +150℃
Voltage on Any Pin with Respect to Ground	-0.5V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

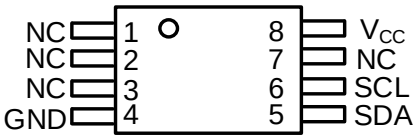
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Packaging Type

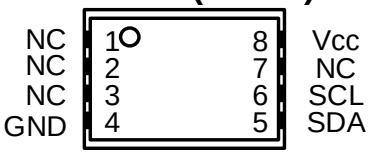
SOP 8



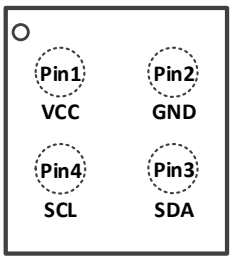
TSSOP8



USON8(2×mm)



Thin 4-ball WLCSP[1] (CTE)



(TOP VIEW)

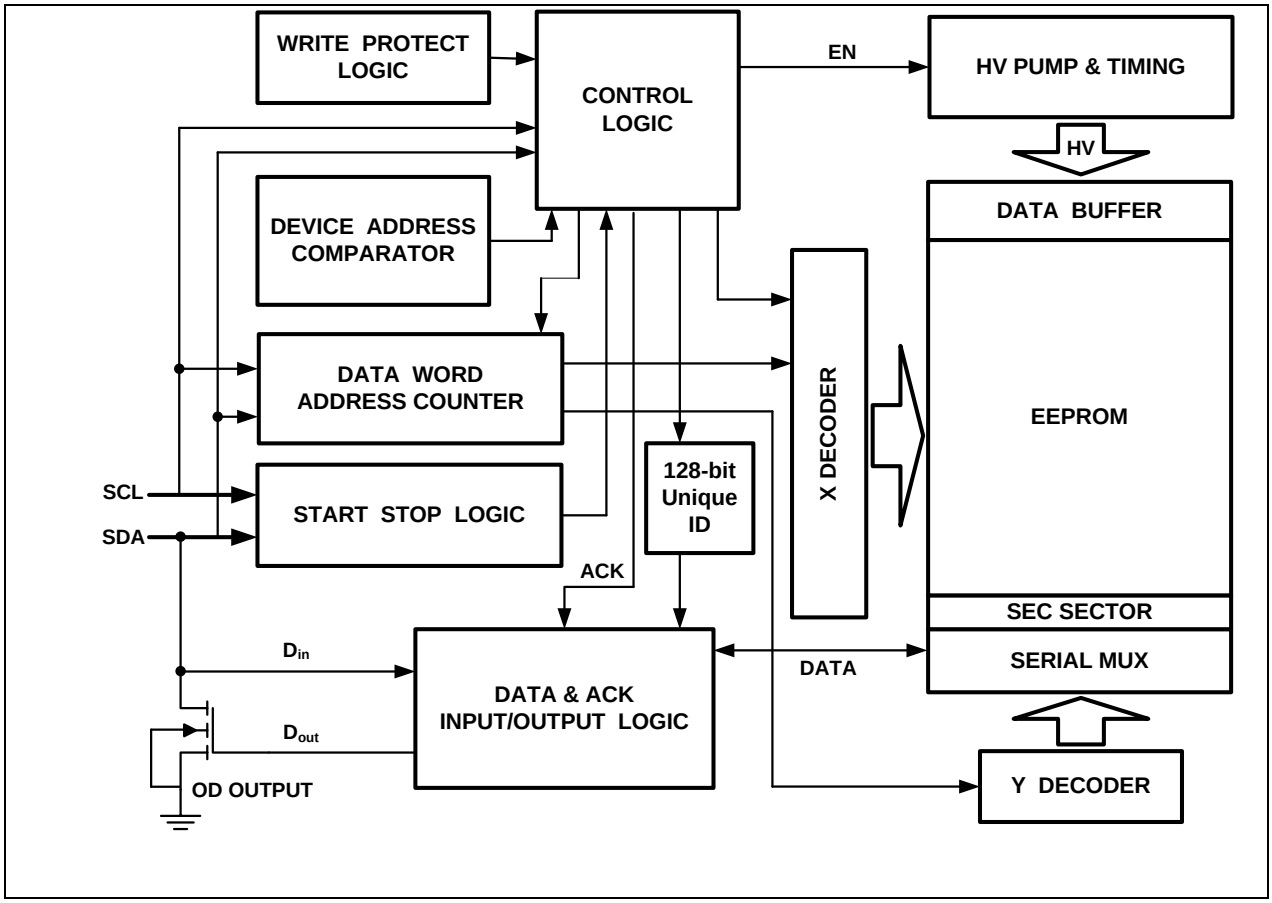
Note:

1. Please contact local sales office for detail description.

Pin Configurations

Pin Name	Function
SDA	Serial Data Input/Output
SCL	Serial Clock Input
V_{CC}	Power Supply
GND	Ground
NC	Not Connect

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Write Protect Description

If precautions are not taken, inadvertent writes may occur during transitions of the host system. The FM24N64 has provided SWP feature that will protect the memory against inadvertent writes. When SWP enabled, the whole memory will be read-only except SWP NVM bit. The SWP feature may be enabled (SWP=1'b) or disabled (SWP=0'b) by the user. The FM24N64 is shipped from FMSH with SWP disabled.

SWP Status	Part of the Memory Protected
SWP=1'b	Full Memory Protected
SWP=0'b	No Protected

Memory Organization

FM24N64, 64K SERIAL EEPROM: Internally organized with 256 pages of 32 bytes each, the 64K requires a 13-bit data word address for random word addressing.

Security Sector: The FM24N64 offers 32-byte Security Sectors which can be written and (later) permanently locked in Read-only mode. This memory may be used by the system manufacturers to store security and other important information separately from the main memory array.

Unique ID: The FM24N64 utilizes a separate memory block containing a factory programmed read-only 128-bit unique ID.

Configurable Device Address (CDA): The FM24N64 provides the CDA features to allow as many as eight devices on the same bus. When power-on, the device will load the device address Configurations automatically. The CDA contains C0/C1/C2/CX four NVM bits. When CX is set to '1b', the device responds to all device address. Otherwise, the device only responds to the same device address as how C2/C1/C0 is set. The CDA factory default value is '0000b'.

WREN:FM24N64 offers a volatile register to protect CDA and SWP bit from unexpected write operation. Before writing CDA and SWP bit, the 'WREN' register must be previously set to 1'b. Because the register will be automatically set to 0'b after any read or write operation, the following command must be a 'Write CDA' command. The default value of 'WREN' register after power-on is 0'b.

Table 1. Memory Organization

Device ADDR	Page ADDR	Byte Number		
		31	…	0
1010	0	Data Memory (256P X 32B)		
	1			
	2			
	…			
	255			
1011	xxxx x00x xxxx xxxx[1]	Security Sector (1P X 32B)		
1011	xxxx x01x xxxx xxxx[2]	128 Bits Unique ID（UID）		
1011	xxxx x10x xxxx xxxx[3]	1 Bit Lock Bit（LB）		
1011	xxx0 0110 1100 1010[4]	Configurable Device Address (CDA) & SWP		
1011	xxx1 1111 0011 0101[5]	WREN		

Note: 1. Address bits ADDR<10:9> must be 00'b, ADDR<4:0> define byte address, other bits are don't care.
2. Address bits ADDR<10:9> must be 01'b, ADDR<3:0> define byte address, other bits are don't care.
3. Address bits ADDR<10:9> must be 10'b, other bits are don't care.
4. Address bits ADDR<12:0> must be 0, 0110, 1100, 1010'b, other bits are don't care.
5. Address bits ADDR<12:0> must be 1, 1111, 0011, 0101'b, other bits are don't care.

Pin Capacitance

SYMBOL	PARAMETER	CONDITIONS	Max	Units
C_{IN}[1]	Input Capacitance	V_{IN} = 0V, f = 1MHz	6	pF
C_{OUT}[1]	Output Capacitance	V_{OUT} = 0V, f = 1MHz	8	pF

Note: 1. This parameter is characterized and is not 100% tested.

Reliability Performance

PARAMETER	SYMBOL	Test Condition	Max	Units
Write cycle endurance (Page Mode)	Ncycle	T_A = 25 °C, $V_{CC(min)}$ < V_{CC} < $V_{CC(max)}$	4,000,000	Write cycle
Data Retention	DR	T_A = 55 °C	100	Year

Note:
1. This parameter is characterized and qualification. It is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_A= -40℃ to +85℃, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Max	Units
V_{CC}	Supply Voltage		1.7	5.5	V
I_{CC1}	Supply Current	V_{CC}=1.7V, Read at 400KHz		0.4	mA
I_{CC2}	Supply Current	V_{CC}=5.5V, Read at 400KHz		0.6	mA
I_{CC3}	Supply Current	V_{CC}= 1.7V, Write at 400KHz		0.7	mA
I_{CC4}	Supply Current	V_{CC}= 5.5V, Write at 400KHz		0.8	mA
I_{SB1}	Standby Current	V_{CC}=1.7V, V_{IN}=V_{CC}/GND		1.0	μA
I_{SB2}	Standby Current	V_{CC}= 5.5V, V_{IN}=V_{CC}/GND		5.0	μA
I_{LI}	Input Leakage Current	V_{IN}=V_{CC}/ GND		1.0	μA
I_{LO}	Output Leakage Current	V_{OUT}=V_{CC}/ GND		1.0	μA
V_{IL}[1]	Input Low Level		-0.5	V_{CC} x 0.3	V
V_{IH}[1]	Input High Level		V_{CC} x 0.7	V_{CC}+0.5	V
V_{OL2}	Output Low Level 2	V_{CC}= 3.0V, I_{OL}=2.1 mA		0.4	V
V_{OL1}	Output Low Level 1	V_{CC}=1.7V, I_{OL}= 0.15 mA		0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

400 kHz AC characteristics

Recommended operating conditions: T_A = -40℃ to +85℃, V_{CC}= +1.7V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.3		μs
t_{HIGH}	Clock Pulse Width High	0.6		μs
t_I[1]	Noise Suppression Time		80	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	μs
t_{BUF}[1]	Time the bus must be free before a new transmission can Start	1.3		μs
$t_{HD.STA}$	Start Hold Time	0.6		μs
$t_{SU.STA}$	Start Setup Time	0.6		μs
$t_{HD.DAT}$	Data In Hold Time	0		μs
$t_{SU.DAT}$	Data In Setup Time	100		ns
t_R	Inputs Rise Time[1]		300	ns
t_F	Inputs Fall Time[1]		300	ns
$t_{SU.STO}$	Stop Setup Time	0.6		μs
t_{DH}	Data Out Hold Time	100		ns
t_{WR}	Write Cycle Time		5	ms

1 MHz AC characteristics

Recommended operating conditions: T_A = -40℃ to +85℃, V_{CC}= +1.7V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		1	MHz
t_{LOW}	Clock Pulse Width Low	500		ns
t_{HIGH}	Clock Pulse Width High	300		ns
t_I[1]	Noise Suppression Time		80	ns
t_{AA}	Clock Low to Data Out Valid	100	450	ns
t_{BUF}[1]	Time the bus must be free before a new transmission can Start	500		ns
$t_{HD.STA}$	Start Hold Time	250		ns
$t_{SU.STA}$	Start Setup Time	250		ns
$t_{HD.DAT}$	Data In Hold Time	0		ns
$t_{SU.DAT}$	Data In Setup Time	50		ns
t_R	Inputs Rise Time[1]		120	ns
t_F	Inputs Fall Time[1]		120	ns
$t_{SU.STO}$	Stop Setup Time	250		ns
t_{DH}	Data Out Hold Time	100		ns
t_{WR}	Write Cycle Time		5	ms

Notes: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:
   RL (connects to V_{CC}): 1.3 kΩ
   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
   Input and output timing reference voltages: 0.5 V_{CC}
   Input rise and fall times: ≤ 50 ns

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure **4**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure **5**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

ACKNOWLEDGE: All address and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

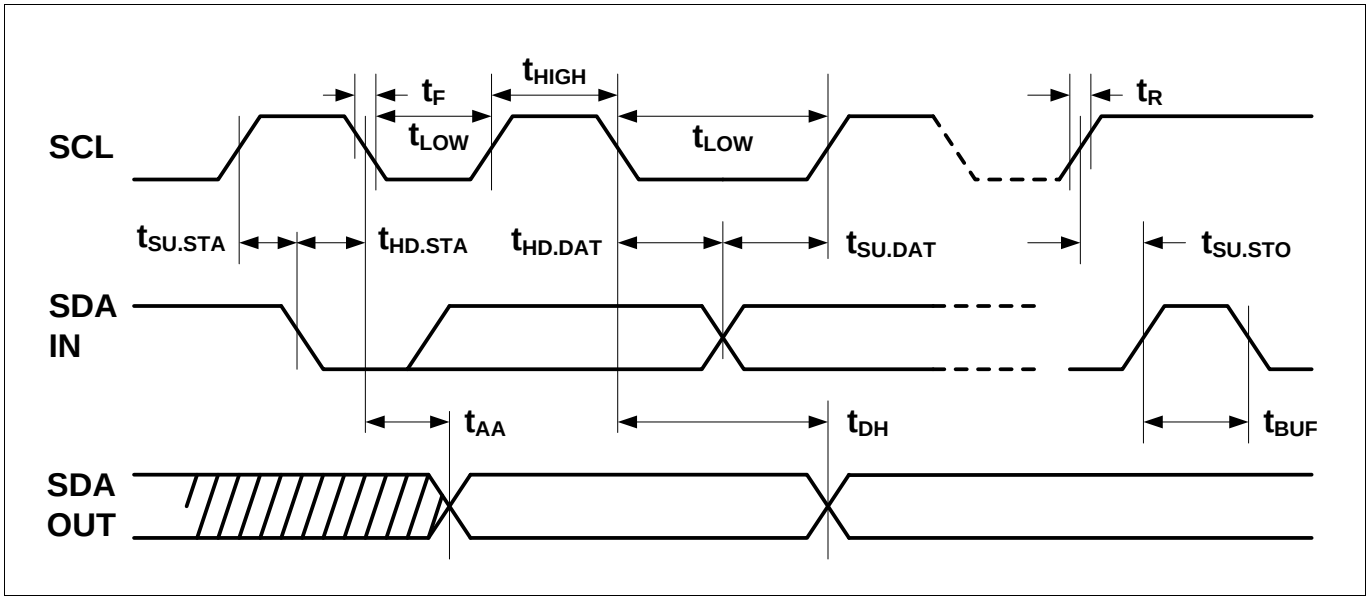
STANDBY MODE: The FM24N64 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

Memory RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset in following these steps:

1. Clock up to 9 Cycles,
2. Look for SDA high in each cycle while SCL is high and then,
3. Create a start condition as SDA is high.

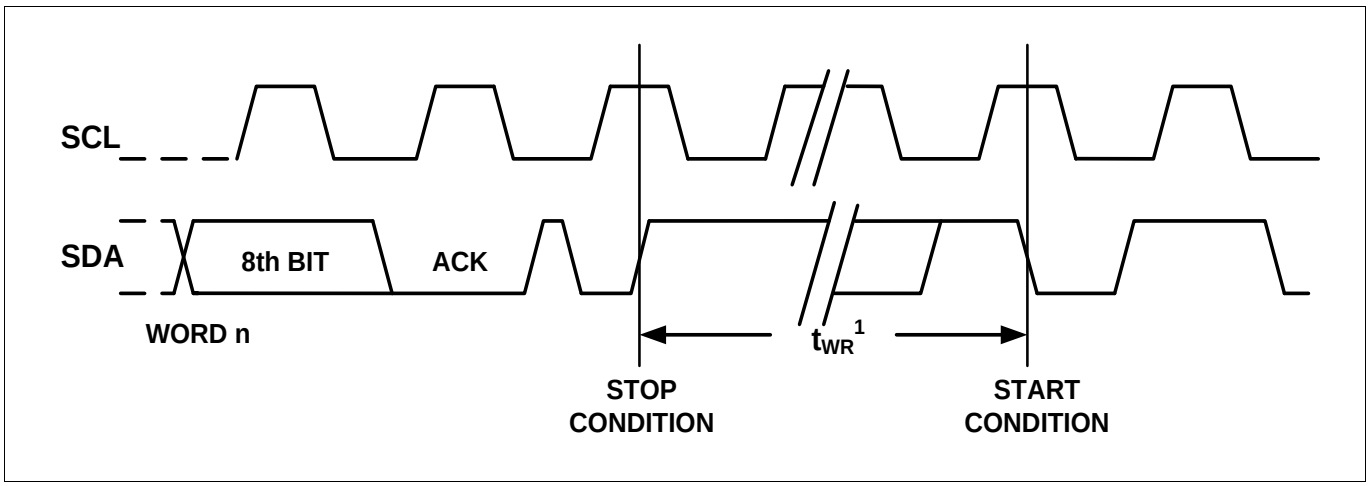
Bus Timing

Figure 2. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 3. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4. Data Validity

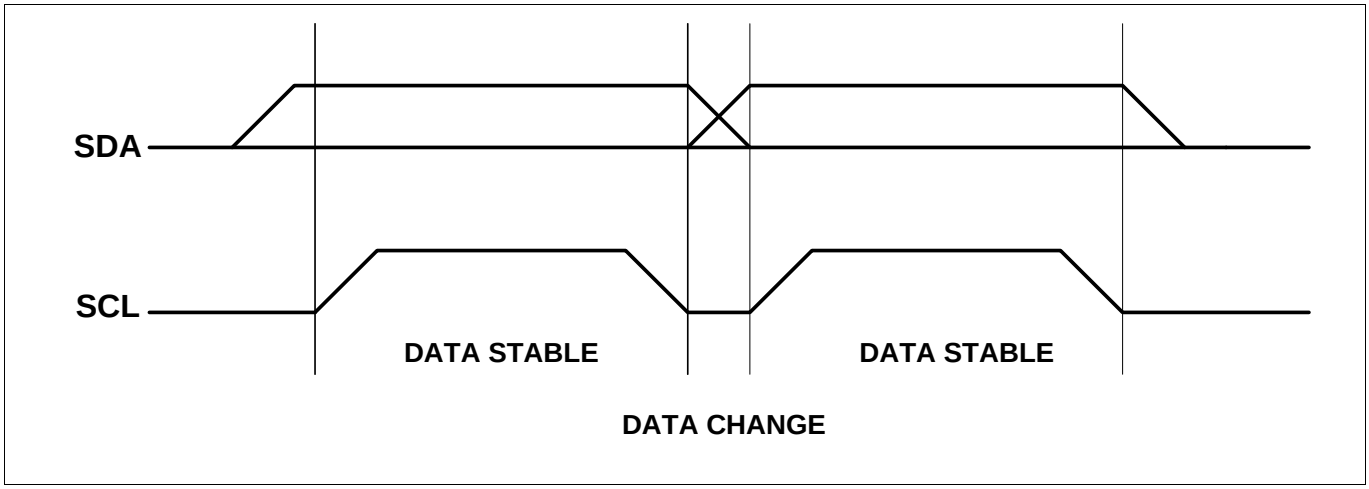


Figure 5. Start and Stop Definition

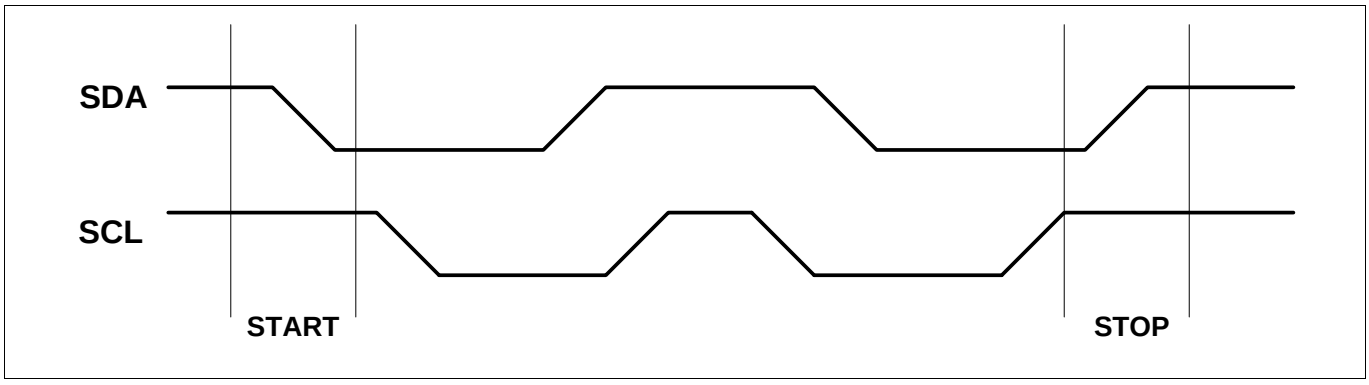
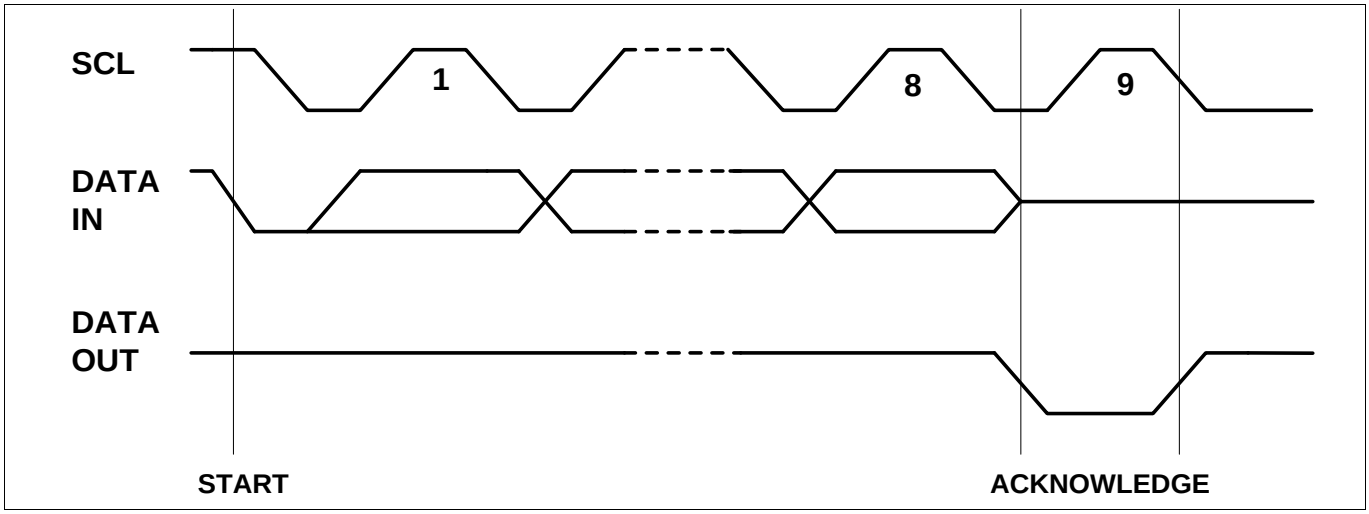
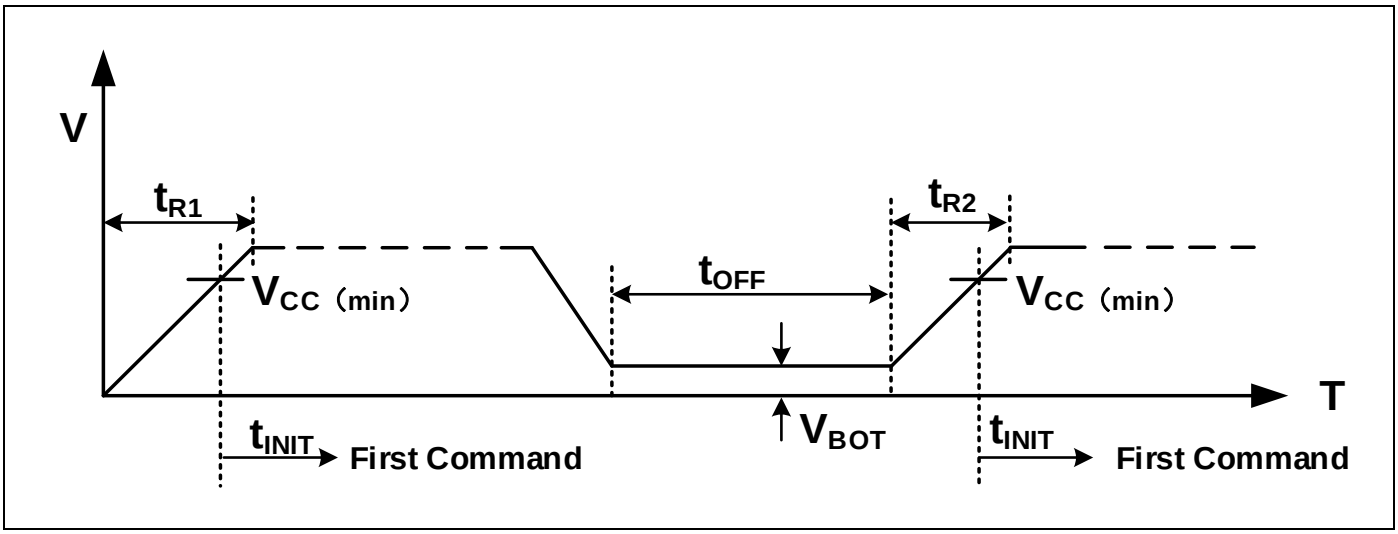


Figure 6. Output Acknowledge



Power-up Timing

Figure 7. V_{CC} Ramp Up and Ramp Down



Symbol	Parameter	Test Condition	Min	Max	Units
t_{R1}	Power on time from 0V			20	ms
t_{R2}	Power on time from V_{BOT}	V_{BOT}≤0.2V		5	ms
t_{OFF}	power cycle off time		50		ms
t_{INIT}	Time from power on to first command		100		us
V_{BOT}	Power Off threshold for the next power on cycle	No ringback above V_{BOT}		0.2	V

Note: VCC must rise monotonically without ringback.

Device Addressing

Data Memory Access: The 64K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Table 2~Table 4).

The device address word consists of a mandatory '1010' (Ah) sequence for the first four most significant bits as shown in Table 2. This is common to all the EEPROM devices.

The FM24N64 provides the Configurable Device Address (CDA) feature. When CX is set to '0b', the 64K EEPROM uses the three device address bits C2, C1, C0 to allow as many as eight devices on the same bus. These bits must compare to C2/C1/C0 bits in Configurable Device Address, refer to 'Memory Organization'. When CX is set to '1b', the device responds to any device address, thus only one device is allowed on each bus.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

Unique ID Access: The FM24N64 utilizes a separate memory block containing a factory programmed 128-bit unique ID. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 2). The behavior of the next three bits (C2/C1/C0) remains the same as during a standard memory addressing sequence.

The eighth bit of the device address needs be set to a one to read the Serial Number. Writing or altering the 128-bit unique ID is not possible.

For more details on accessing this special feature, See Read Operations on page 15.

Security Sector Access: The FM24N64 offers 32-byte Security Sector which can be written and (later) permanently locked in Read-only mode. Access to this memory location is obtained by beginning the device address word with a '1011' (Bh) sequence (refer to Table 2). The behavior of the next three bits (C2/C1/C0) remains the same as during a standard memory addressing sequence.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

For more details on accessing this special feature, See Write Operations and Read Operations on page 13-15.

CDA and SWP Access: Access to this memory location is obtained by beginning the device address word with a '1011b' (Bh) sequence (refer to Table 2). The behavior of the next three bits (C2/C1/C0) remains the same as during a standard memory addressing sequence.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

For more details on accessing this special feature, See Write Operations and Read Operations on page 13-15.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device.

DATA SECURITY: FM24N64 has provided SWP feature that will protect the memory against inadvertent writes. When SWP enabled, the whole memory will be read-only except SWP NVM bit. The SWP feature may be enabled (SWP=1'b) or disabled (SWP=0'b) by the user. The FM24N64 is shipped from FMSH with SWP disabled.

Table 2. Device Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	1	0	1	0	C2	C1	C0	R/W
Security Sector	1	0	1	1	C2	C1	C0	R/W
Security Sector Lock Bit	1	0	1	1	C2	C1	C0	R/W
Unique ID Number	1	0	1	1	C2	C1	C0	1
CDA and SWP	1	0	1	1	C2	C1	C0	R/W
WREN	1	0	1	1	C2	C1	C0	0
	MSB							LSB

Table 3. First Word Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	x	x	x	A12	A11	A10	A9	A8
Security Sector	x	x	x	x	x	0	0	x
Security Sector Lock Bit	x	x	x	x	x	1	0	X
Unique ID Number	x	x	x	x	x	0	1	x
CDA and SWP	x	x	x	0	0	1	1	0
WREN	x	x	x	1	1	1	1	1
	MSB							LSB

NOTE: x = Don`t care bit.

Table 4. Second Word Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	A7	A6	A5	A4	A3	A2	A1	A0
Security Sector	x	x	A5	A4	A3	A2	A1	A0
Security Sector Lock Bit	x	x	x	x	x	x	x	x
Unique ID Number	x	x	x	x	0	0	0	0
CDA and SWP	1	1	0	0	1	0	1	0
WREN	0	0	1	1	0	1	0	1
	MSB							LSB

NOTE: x = Don`t care bit.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, $t_{WR,}$ to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8).

PAGE WRITE: The 64K EEPROM is capable of 32-byte page writes. A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 9).

The data word address lower seven bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

WRITE SECURITY SECTOR: Write the Security Sector is similar to the page write but requires use of device address, and the special word address seen in Table 2-Table 4 on page 12. The higher address bits ADDR<15:5> are don’t care except for address bits ADDR<10:9>，which must be equal to ‘00b’. Lower address bits ADDR<4:0> define the byte address inside the Security Sector (see Figure 13).

If the Security Sector is locked, the data bytes transferred during the Write Security Sector operation are not acknowledged (NoAck).

LOCK SECURITY SECTOR: Lock the Security Sector is similar to the byte write but requires use of device address, and special word address seen in Table 2-Table 4 on page 12. The word address bits ADDR<10:9> must be ‘10b’, all other word address bits are don’t care. The data byte must be equal to the binary value xxxx xx1x, where x is don't care (see Figure 15).

If the Security Sector is locked, the data bytes transferred during the Lock Security Sector operation are not acknowledged (NoAck).

WREN:
The FM24N64 offers a volatile register to protect CDA & SWP bit from unexpected write operation. Before writing CDA and SWP, the ‘WREN’ register must be previously set to 1. Because the register will be automatically set to 0 after any read or write operation, the following command must be a ‘Write CDA’ command. The default value of ‘WREN’ register after power-on is 0b.

Write the ‘WREN’ register is similar to the page write but requires use of device address, and the special word address seen in Table 2-Table 4 on page 12. The word address bits ADDR<12:0> must be ‘1, 1111, 0011, 0101b’, and ADDR<15:13> is don’t care. After the word address bytes, the register will be set and will be cleared after next command. That is, a following WRITE CDA and SWP command should be performed. For ‘WREN’ is a volatile register, no write cycle time is needed in this command (see Figure 18).

WRITE CDA & SWP: Before writing CDA & SWP, a previously 'WREN' command must be performed. Write CDA & SWP operation is similar to the byte write but requires use of device address, and specific word address. The word address bits ADDR<12:0> must be '0, 0110, 1100, 1010b' (see Table 3-Table 4), and ADDR<15:13> is don't care. The data byte must be equal to the binary value 'C2C1C0CXxxSWPx' (see Table 5 and Figure 19).

CDA and SWP NVM Bit defined as following Table 5:

Table 5. CDA and SWP NVM Bit

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C2	C1	C0	CX	x	x	SWP	x
MSB							LSB

NOTE: x = Don`t care bit.

Refer to ordering information on page 21 for the CDA factory default value. The SWP bit default value is '0b' (SWP disabled). CDA could be configured when SWP is disabled. If SWP is disabled, CDA and SWP could be re-configured in the same write operations. Once CDA re-configured, the following command with device address bits must be in accordance with the modified CDA, otherwise the device will return to standby state. If SWP is enabled, CDA is protected by SWP. CDA can't be modified even during the SWP disable operation, the value of CDA (C2'/C1'/C0'/ CX') in DATA0 of write CDA & SWP command sequence is ignored.

Note:

1. The CDA status could be checked by Ack polling. There will be an Ack when C2C1C0 value in device addresses of command sequence is correct according to CDA, otherwise NoAck.
2. Write CDA & SWP operation do not support Ack polling to check whether the internal write cycle has completed. The next instruction issuing must wait for the end of the internal write cycle(t_{WR}(max)=5ms), otherwise the instruction is invalid.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 10).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 12).

UNIQUE ID READ: Reading the serial number is similar to the sequential read but requires use of the device address, a dummy write, and the use of specific word address seen in Table 2-Table 4 on page 12. The higher address bits ADDR<15:4> are don't care except for address bits ADDR<10:9>，which must be equal to '01b'. Lower address bits ADDR<3:0> define the byte address inside the UID. If the application desires to read the first byte of the UID, the lower address bits ADDR<3:0> would need to be '0000b'.

When the end of the 128-bit UID number is reached (16 bytes of data), the data word address will roll-over back to the beginning of the 128-bit UID number. The Unique ID Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 17).

READ SECURITY SECTOR：Read the Security Sector is similar to the random read but requires use of device address, a dummy write, and the use of specific word address seen in Table 2-Table 4 on page 12. The higher address bits ADDR<15:5> are don't care except for address bits ADDR<10:9>， which must be equal to '00b'. The lower address bits ADDR<4:0> define the byte address inside the Security Sector.

The internal byte address is automatically incremented to the next byte address after each byte of data is clocked out. When the last byte (1Fh) is reached, it will roll over to 00h, the first byte of the Security Sector, and continue to increment. (see Figure 14).

READ LOCK STATUS：There are two ways to check the lock status of the Security Sector.
1. The first way is initiated by a Security Sector Write, the EEPROM will acknowledge if the Security Sector is unlocked, while it will not acknowledge if the Security Sector is locked.
Once the acknowledge bit is read, it is recommended to generate a Start condition followed by a Stop condition, so that:

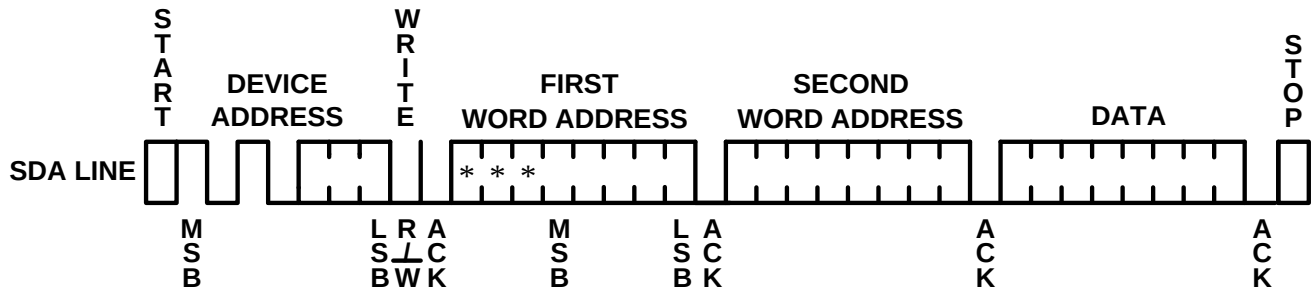
- Start: the truncated command is not executed because the Start condition resets the device internal logic
- Stop: the device is then set back into Standby mode by the Stop condition.

2. The second way is initiated by a Lock Status Read. Lock Status Read is similar to the random read but requires use of device address seen in Table 2-Table 4 on page 12, a dummy write, and the use of specific word address. The address bits ADDR<10:9> must be '10b', all other address bits are Don't Care. The Lock bit is the BIT1 of the byte read on SDA. It is at "1" when the lock is active and at "0" when the lock is not active. The same data is shifted

out repeatedly until the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 16).

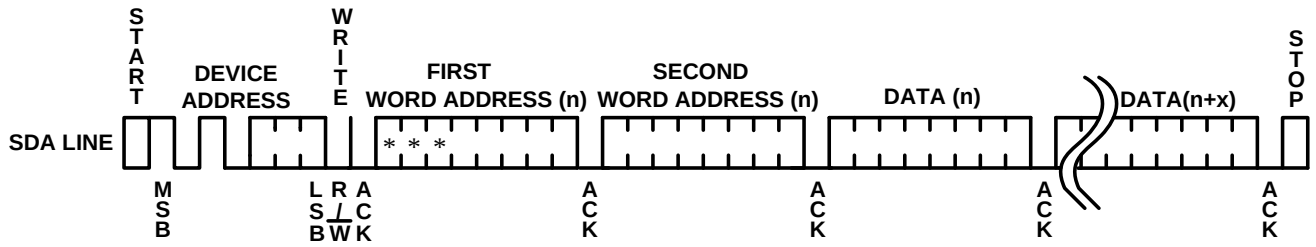
READ CDA & SWP: Read CDA & SWP operation is similar to the random read but requires use of device address, a dummy write, and specific word address. The word address bits ADDR<12:0> must be '0, 0110, 1100, 1010b' (see Table 2-Table 4), and ADDR<15:13> is don't care. The CDA is the BIT7~BIT4 of the byte read on SDA, and SWP is the BIT1, other bits are don't care. The internal byte address is not automatically incremented, so the same data is shifted out repeatedly until the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 20).

Figure 8. Byte Write



Note: 1. * = *Don't CARE* bits

Figure 9. Page Write



Note: 1. * = *Don't CARE* bits

Figure 10. Current Address Read

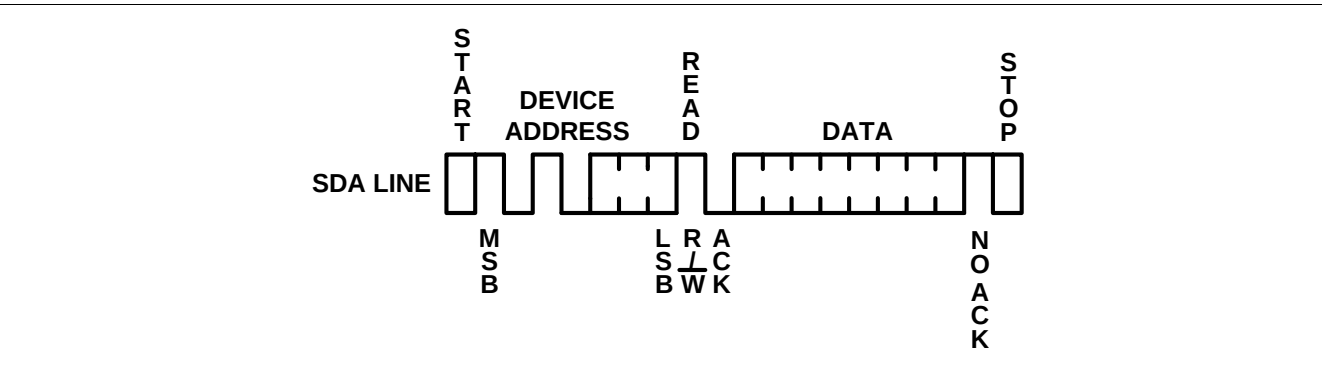
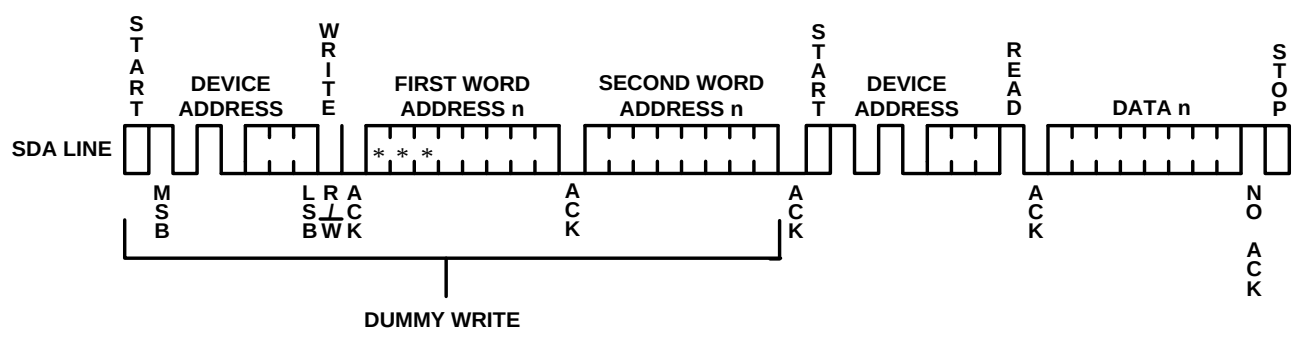


Figure 11. Random Read



Note: 1. * = *Don't CARE* bits.

Figure 12. Sequential Read

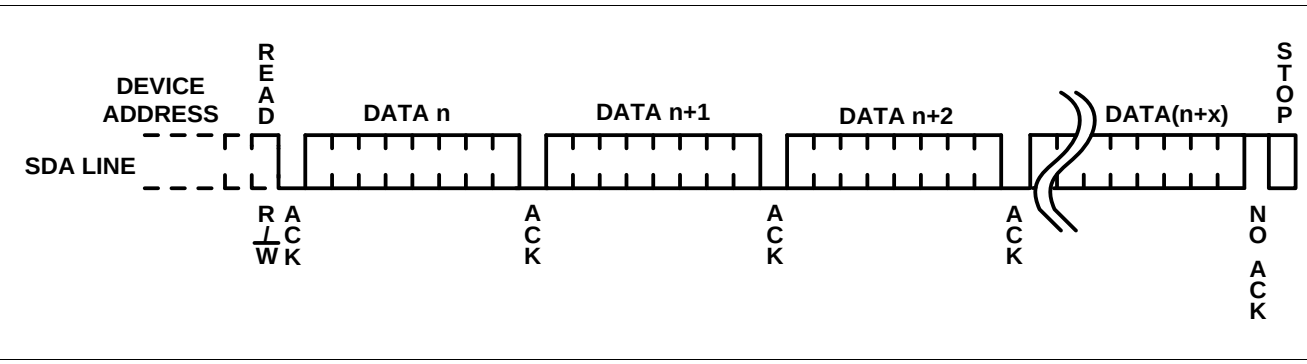
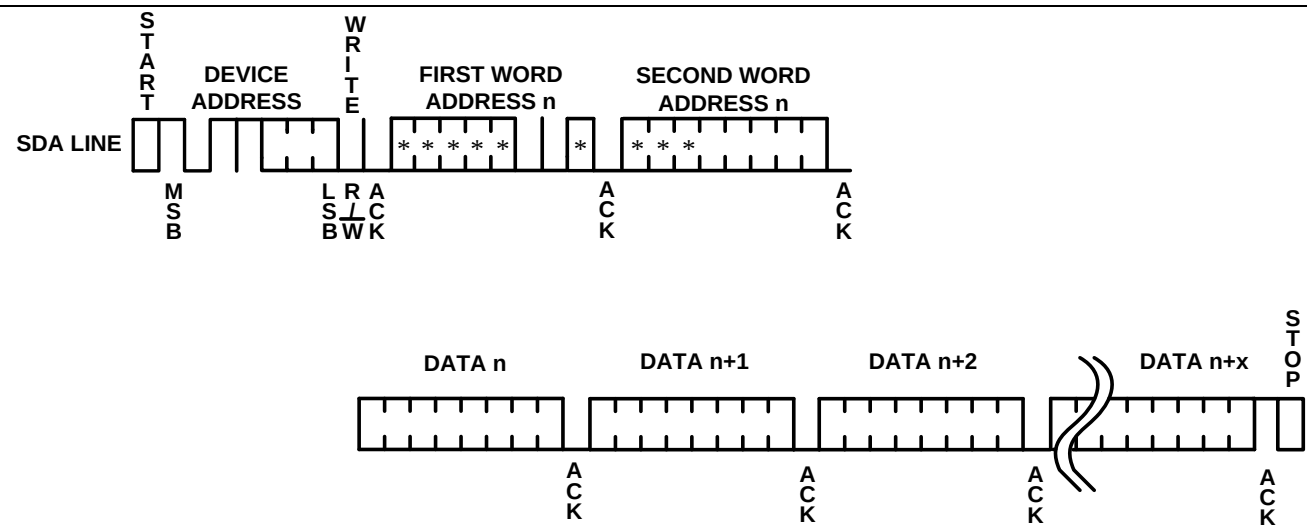
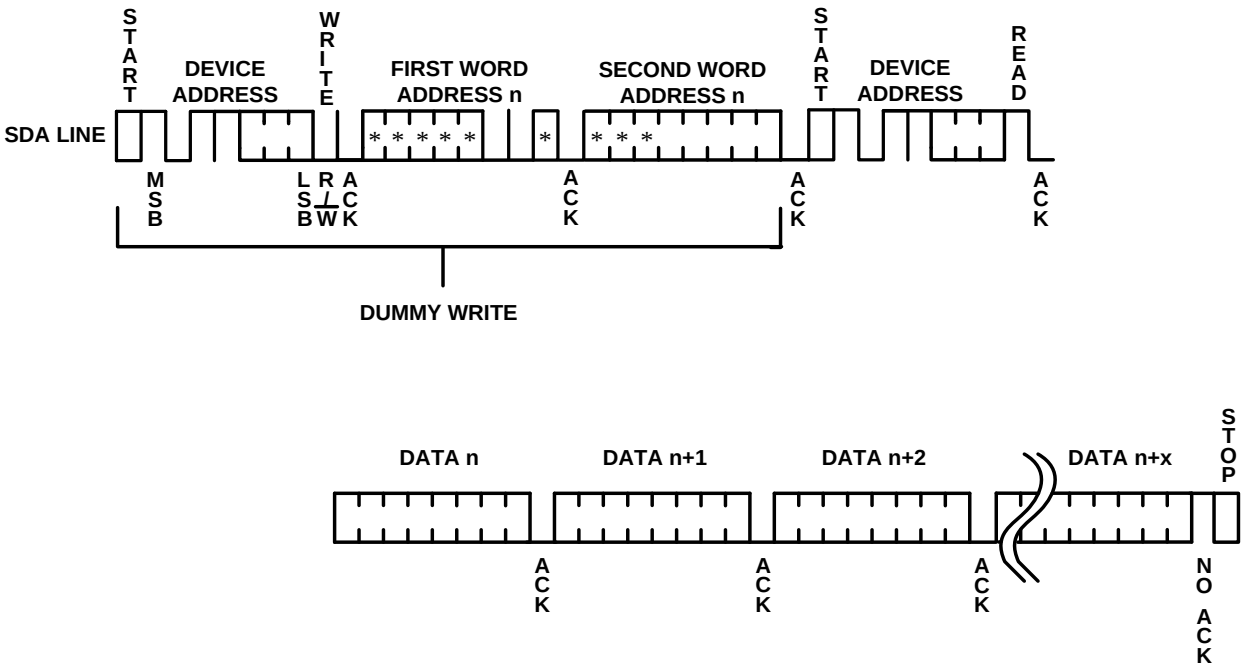


Figure 13. Write Security Sector



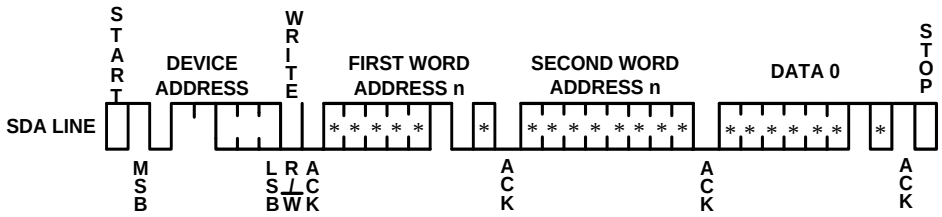
Note: 1. * = *Don't CARE* bits.

Figure 14. Read Security Sector



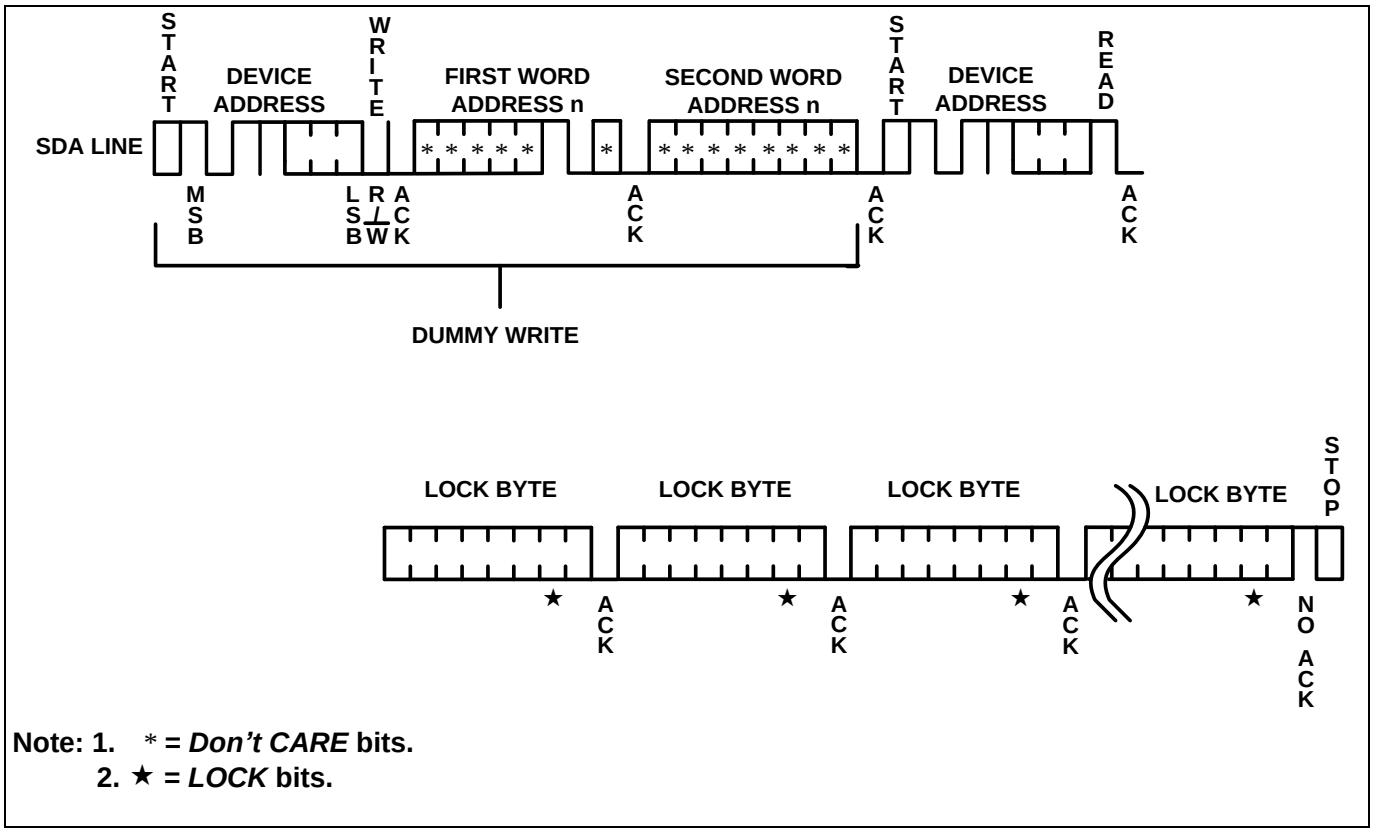
Note: 1. * = *Don't CARE* bits.

Figure 15. Lock Security Sector



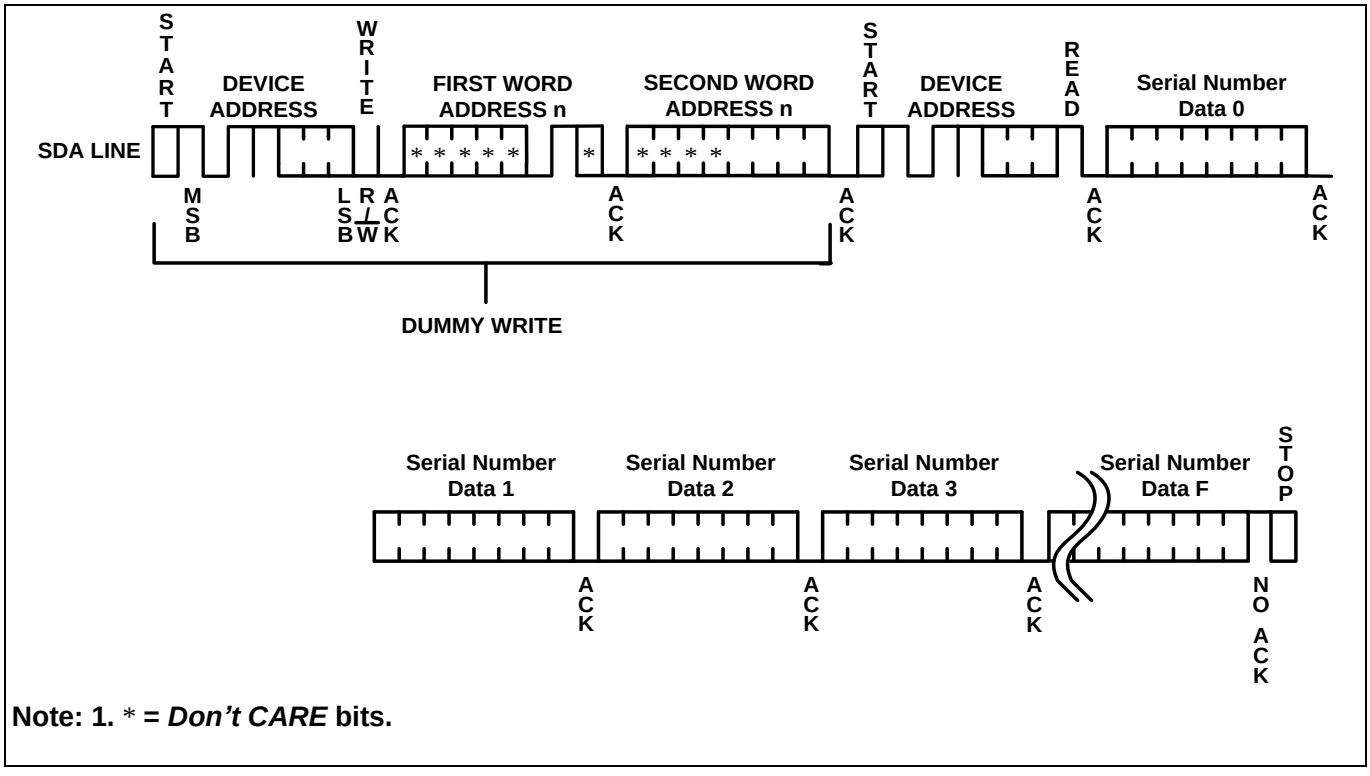
Note: 1. * = *Don't CARE* bits.

Figure 16. Read Lock Status



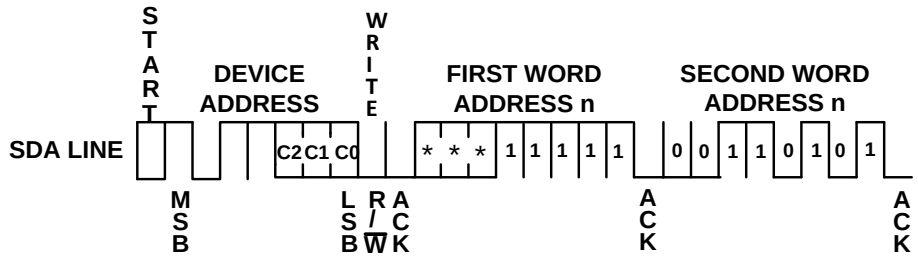
Note: 1. * = *Don't CARE* bits.
2. ★ = *LOCK* bits.

Figure 17. Read Unique ID



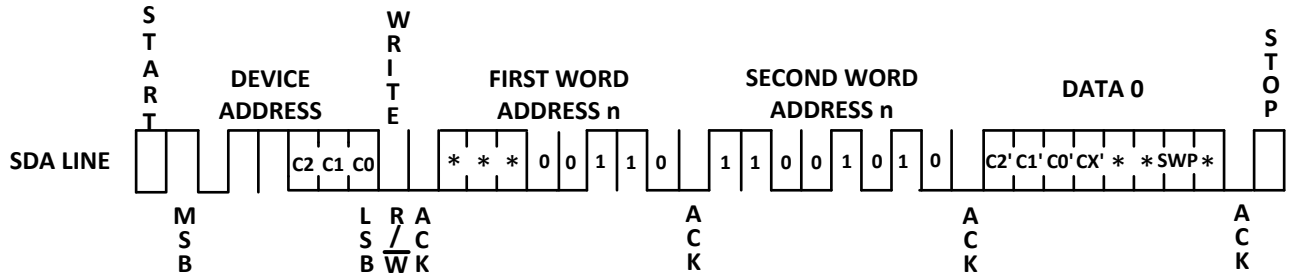
Note: 1. * = *Don't CARE* bits.

Figure 18. WREN



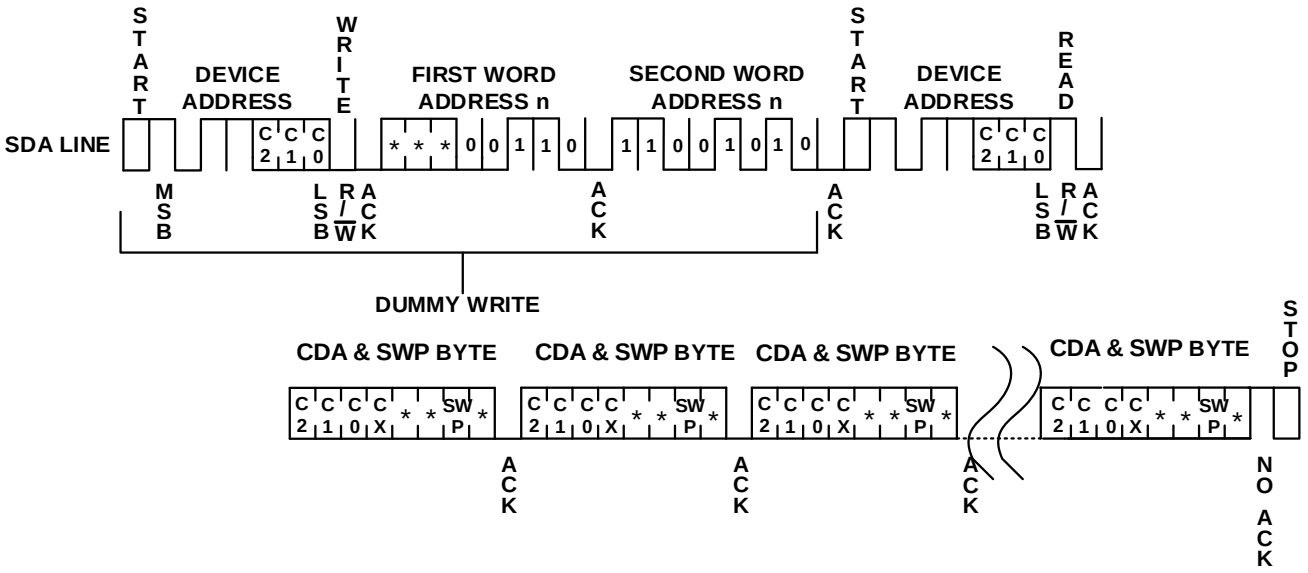
Note: 1. * = *Don't CARE* bits.

Figure 19. Write CDA & SWP



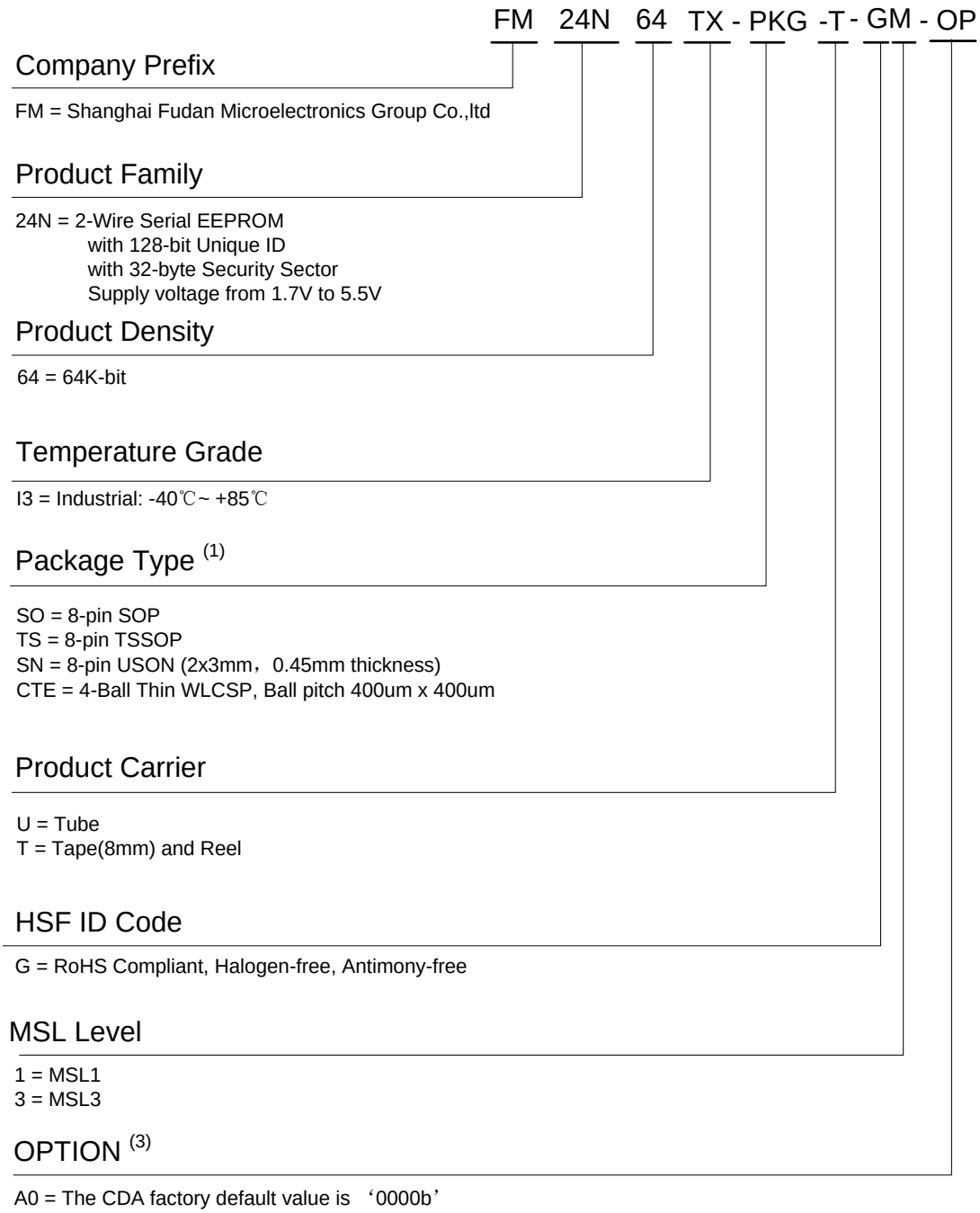
Note: 1. * = *Don't CARE* bits.
2. C2'/C1'/C0'/CX'/SWP'= the new value of CDA & SWP

Figure 20. Read CDA & SWP



Note: 1. * = *Don't CARE* bits.

Ordering Information

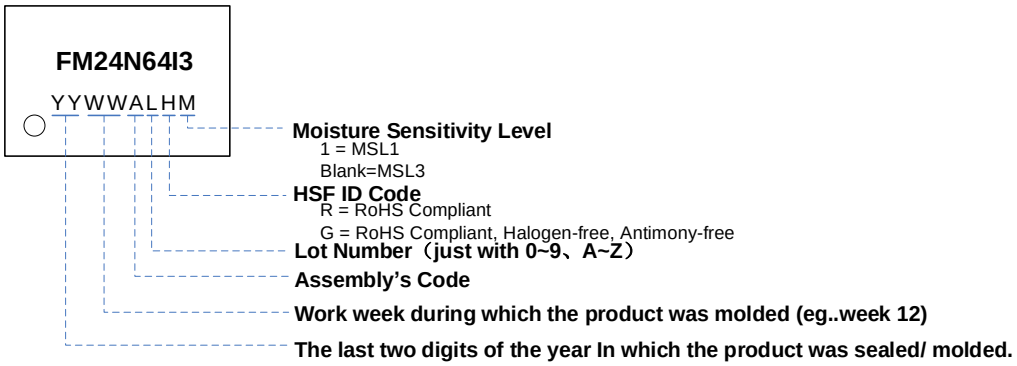


Note:

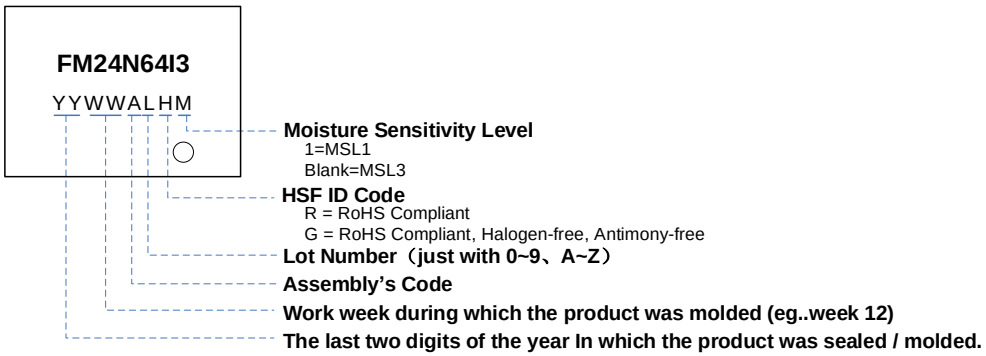
1. For SO package, MSL1 package are available, for detail please contact local sales office. For WLCSP package please contact local sales office.
2. For other configuration, please contact local sales office.

Part Marking Scheme

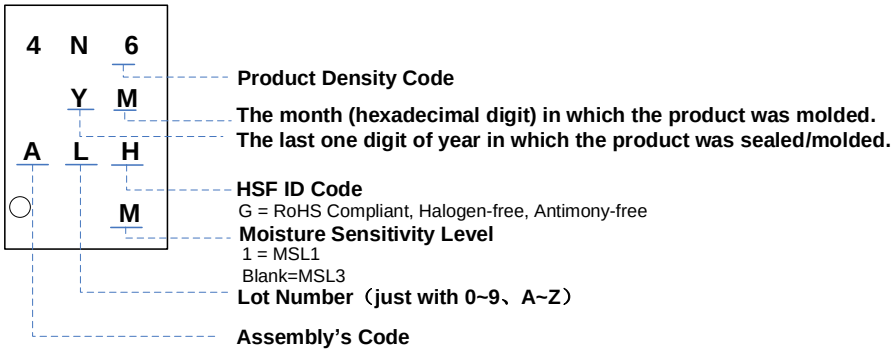
SOP8



TSSOP8

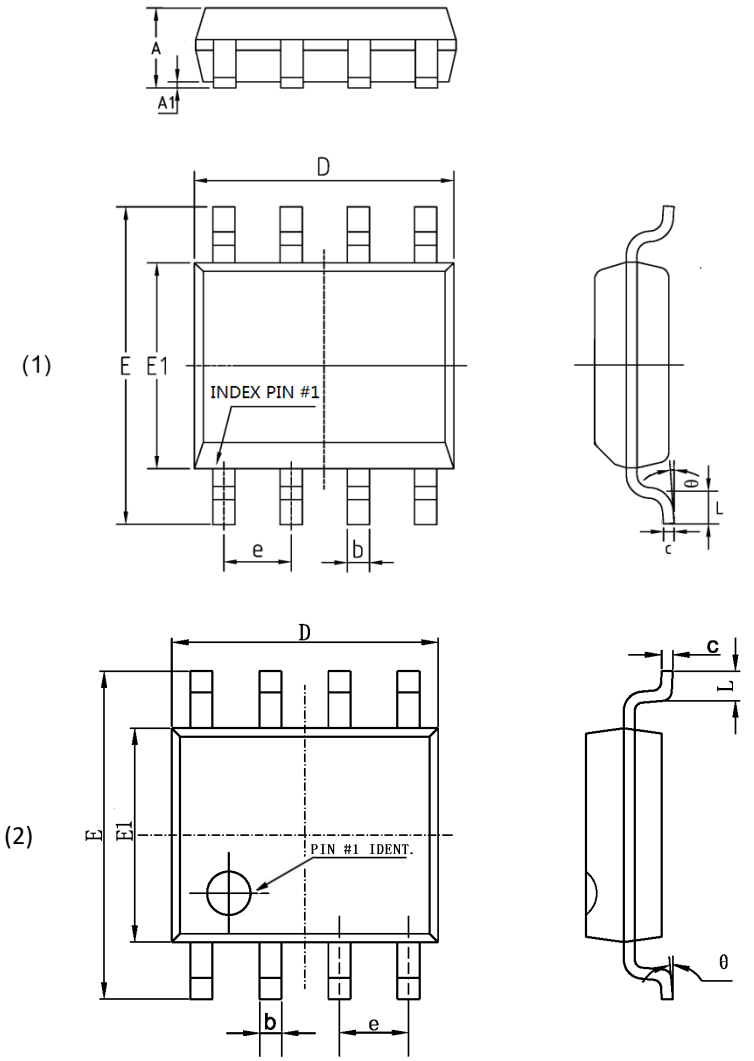


USON8



Packaging Information

SOP 8

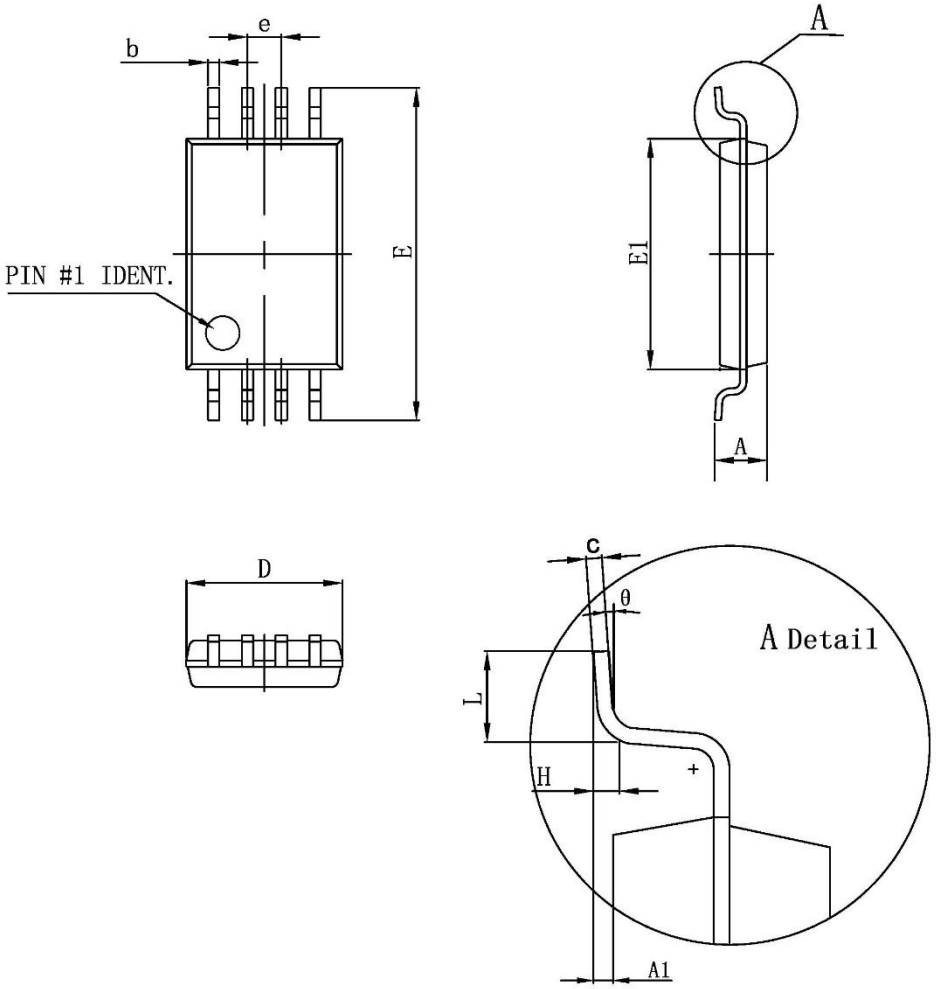


Symbol	MIN	NOM	MAX
A	1.350	1.550	1.750
A1	0.050	0.150	0.250
b	0.330	0.420	0.510
c	0.150	0.200	0.250
D	4.700	4.925	5.150
E1	3.700	3.900	4.100
E	5.800	6.000	6.200
e		1.270(BSC)	
L	0.400	0.650	0.900
θ	0°	4°	8°

NOTE:

1. **Dimensions are in Millimeters.**

TSSOP8

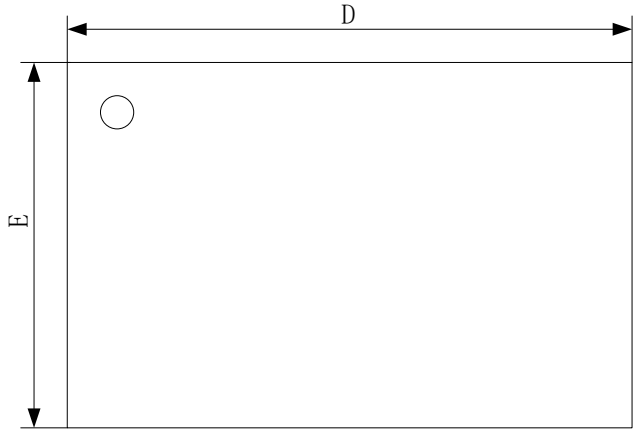


Symbol	MIN	NOM	MAX
D	2.900	3.000	3.100
E1	4.300	4.400	4.500
b	0.190	0.245	0.300
c	0.090	0.145	0.200
E	6.200	6.400	6.600
A	–	-	1.200
A1	0.050	0.100	0.150
e	0.650 (BSC)		
L	0.450	0.600	0.750
θ	0°	4°	8°

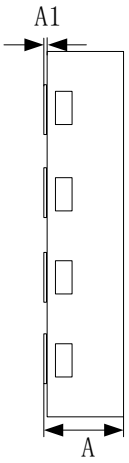
NOTE:

1. **Dimensions are in Millimeters.**

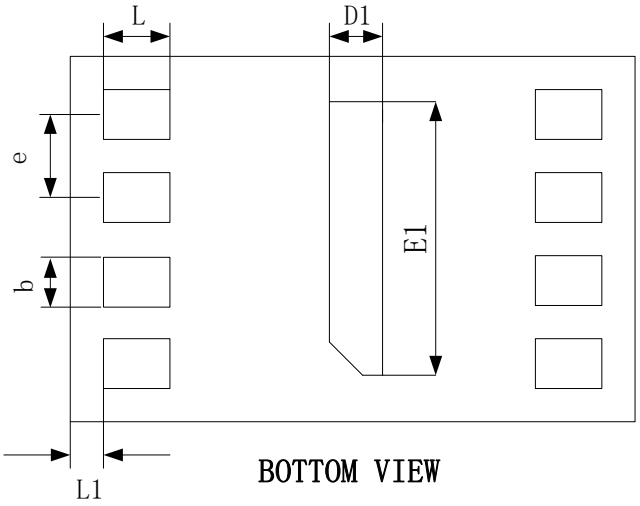
USON8(2x3mm, 0.45mm thickness)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	MIN	NOR	MAX
A	0.400	0.450	0.500
A1	0.000	0.025	0.050
D	2.900	3.000	3.100
E	1.900	2.000	2.100
D1	0.100	0.200	0.300
E1	1.500	1.600	1.700
b	0.200	0.250	0.300
e		0.500(BSC)	
L	0.300	0.350	0.400
L1	0.050	0.100	0.150

NOTE:

1. **Dimensions are in Millimeters.**

Revision History

Version	Publication date	Pages	Revise Description
1.0	Jan. 2023	27	Initial document Release.
1.1	May. 2023	27	1.Removed TDFN Package, added USON Package. 2.Updated the chapters of Packaging type, Ordering information, Part marking scheme and packaging information. 3.Update Isb2 and ti parameters.
1.2	Jul. 2023	27	1.Updated “Ordering Information” 2.Updated “Packaging Information”.
1.3	Oct. 2023	27	1.Updated “Ordering Information”
1.4	Oct. 2024	27	1.Updated “Ordering Information” 2.Updated “Packaging Information”.

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